FORMATION AND PROPERTIES OF NANOMETER-THICK PLATINUM SILICIDE LAYERS

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To

my coming baby

And *in memoriam* to

Thereza Trancucci Capopiza

and

André Conforto

Fini, c'est fini, ça va finir, ça va peut-être finir...

S. Beckett, 'Fin de Partie'

Abstract

Platinum silicide films are widely used in silicon devices for ohmic and Schottky contacts. It has been demonstrated in the recent years that Schottky barriers employing ultra-thin platinum silicide films (thickness < 10 nm) are useful for photodetection in the near infrared.

We have studied the formation of thin platinum silicide films and their electrical properties as a function of the annealing temperature in presence of an interfacial native silicon oxide layer and with plasma etching damage on the Si substrate surface. The thickness of the interfacial oxide layer was varied as well as the depth of the plasma etching damage. The interest of these investigations lies in understanding the role played by the imperfections due to the two usual cleaning processes, namely incomplete SiO_2 chemical removal and Si damace due to plasma etching bombardment, on the final silicide film characteristics.

The quality and reproducibility of platinum silicide films in routine fabrication depends strongly of the process control, where the substrate cleanliness plays a crucial role. The native silicon oxide can be present at the silicon substrate surface due to an incomplete chemical etching or due to the rapid re-growth of the oxide after the chemical etching. It is well accepted that this interfacial oxide layer can cause problems for Pt-contact metallization, although the characteristics of the resulting platinum silicide film as a function of the oxide thickness and the annealing temperature are not well known. On the other hand, to guarantee the complete removal of the native silicon oxide mainly in the delicate ultra-thin silicide films fabrication, a plasma etching bombardment is performed on the substrate surface prior to metal deposition. This can introduce a certain amount of damage in the substrate surface which can influence the Pt-Si reaction as well as the morphology, crystallography and electrical characteristics of these films.

We prepared samples using different chemical etching procedures to obtain complete and incomplete native oxide layer removal. Plasma etching on the substrate surface was performed for various duration and using a range of discharge powers to obtain different plasma etching damage depth. The silicidation reaction was performed at different annealing temperatures. Five characterization techniques were used to study these samples: Transmission Electron Microscopy (TEM), Scanning Electron Microscopy (SEM), Photoelectron Microscopy (PEM), Internal Photoemission (IPE) and Four-Point Probe Measurements. Morphological, compositional, structural and crystallographic information is obtained from the first three techniques. This is subsequently correlated to the electrical properties of the films obtained using the last two techniques.

We observe that silicide films with interfacial oxide layer up to 2.2 nm-thick, annealed at an appropriate temperature, are equivalent to oxide-free samples for application in device metallization. Resistivity measurements show the same minimum value of 30 $\mu\Omega$cm, for samples with and without interfacial oxide in the 350 - 550 °C annealing temperature range.

The role played by the interfacial native oxide layer is observed during the early stages of Pt - Si formation. In the absence of the interface oxide, platinum silicide can easily form even at low temperatures (T < 200 °C). If the interfacial oxide is present, the reactant interdiffusion proceeds through the oxide pinholes; the Pt-Si reaction rate and the phase formation mostly depend on the pinhole density and diameter. In the 350 - 550 °C annealing temperature range, silicide films with and without interfacial oxide layer reach a stable, homogeneous and quite similar structure, consisting of epitaxial and polycrystalline PtSi grains and a very flat silicide/Si interface. This annealing temperature range gives crystallographic and morphollogic conditions in which silicide films with and without interfacial oxide layer show the best transport properties.

Silicide films with an interfacial oxide show a continuous Pt_2Si sub-layer on the top. It is observed from 350 °C and remains unchanged up to annealing temperatures as high as 600 - 650 °C. The existence of this sub-layer can guarantee the film continuity up to 700 °C, even if PtSi grains below it are already epitaxial and isolated from each other. In oxide-free samples this layer does not exist and the transformation to an island-type film is observed after annealing at 550 - 600 °C. The presence of the Pt_2Si layer is beneficial and even desirable for preserving the transport properties.

A few nanometers of plasma etching damage on the substrate surface are beneficial to ultra-thin (3 - 5 nm-thick) silicide films. Plasma damage contributes to slowing down the beginning of the island formation and extends the temperature range in which platinum silicide films maintain their continuity and the transport properties. Plasma damage can slightly increase the resistivity of films in the 4 - 5 nm thickness range. On the other hand, the plasma etching damage depth in the range mentioned above can help films thinner than 3.5 nm to improve their transport properties.

Résumé

Les films de siliciure de platine sont largement employés sur des dispositifs électroniques en silicium comme contacts ohmiques ou Schottky. L'utilité des films ultra-minces de siliciure de platine (épaisseur < 10 nm) dans la fabrications de barrières de Schottky pour la photodétection dans l'infrarouge proche a été souvent démontrée pendant les dernières années.

La qualité des films de siliciure et la reproductibilité de leurs propriétés dans la fabrication de routine dépendent fortement du contrôle du processus, et notamment de la propreté du substrat qui joue un rôle fondamental. Le substrat de silicium est soumis à un nettoyage chimique avant la déposition du film métallique. L'obtention du film de siliciure se fait par réaction thermique entre un film métallique déposé par pulvérisation cathodique ('sputtering') et le substrat. Des résidus d'oxyde natif de silicium peuvent être trouvés à la surface du substrat à cause d'une attaque chimique incomplète ou de la recroissance rapide de la couche d'oxyde natif après l'attaque. Dans les deux cas, l'oxyde de silicium natif peut être la cause de problèmes de métallisation du contact de platine. Cependant les caractéristiques du film de siliciure obtenus en fonction de l'épaisseur de la couche d'oxyde et de la température de recuit ne sont pas bien connues. D'autre part, pour assurer l'élimination complète de l'oxyde natif de silicium, surtout pendant la délicate fabrication des couches ultra-minces de siliciure (épaisseur < 10 nm), un nettoyage plasma est souvent appliqué à la surface du substrat avant la déposition du métal. Cette procédure peut introduire une certaine quantité de dégâts sur la surface du substrat, ce qui influence la réaction Pt-Si ainsi que la morphologie, la cristallographie et les caractéristiques électriques des films de siliciure.

Nous avons étudié la formation de couches minces de siliciure de platine et leurs propriétés électriques en fonction de l'épaisseur de l'oxyde de silicium natif interfacial et de la température de recuit. Nous avons aussi étudié l'influence des dégâts d'irradiation crées par le plasma sur le substrat de silicium en fonction de la température de recuit. Le but de ces investigations est la compréhension du rôle joué par les imperfections dues aux deux processus de nettoyage (oxyde résiduel dû à l'attaque chimique incomplète et dégâts d'irradiation sur le substrat dû au bombardement plasma) sur les caractéristiques morphologiques, structurales et électriques des films de siliciure de platine.

Nous avons préparé des échantillons utilisant différentes procédures d'attaque chimique pour obtenir une élimination complète ou incomplète de la couche d'oxyde natif. Le nettoyage plasma sur la surface du substrat a été effectué pendant des durées variables et en utilisant toute une gamme des puissance de décharge pour obtenir des différentes profondeurs des dégâts. La réaction de siliciuration s'est déroulée à différentes températures de recuit. Cinq techniques de caractérisation ont été utilisées pour étudier ces échantillons: la microscopie électronique à transmission (TEM), la microscopie électronique à balayage (SEM), la microscopie des photoélectrons (PEM), la photoémission interne (IPE) et la mesure de résistivité par quatre points. Les trois premières techniques fournissent des informations sur la morphologie, composition et structure des films qui sont ensuite corrélées aux propriétés électriques étudiées par les deux dernières techniques.

Nous avons observé que les couches de siliciure avec un oxyde interfacial jusqu'à 2.2 nm d'épaisseur, recuites à une température adéquate, sont équivalente à celles sans oxyde pour des applications telle que métallisation de dispositifs en silicium. Les mesures donnent une même valeur de 30 μΩcm pour les échantillons avec et sans oxyde interfacial recuits entre 350-550 °C.

Le rôle joué par l'oxyde natif interfacial peut être observé déjà pendant la première étape de la réaction Pt - Si. En absence d'oxyde interfacial, la formation du siliciure de platine est observée à T = 165 °C déjà. En présence d'oxyde interfacial, la vitesse de la réaction Pt-Si est contrôlée par la diffusion du platine et du silicium au travers des pores du film d'oxyde. La séquence de formation des phases dépend surtout de la densité de pores et de leur diamètre. Entre 350 et 550 °C, les films de siliciure avec ou sans oxyde interfacial atteignent une structure similaire, continue, stable et homogène, qui est formée par un mélange de grains de PtSi épitaxiaux par rapport au substrat de Si[100] et d'autres grains polycristallins. L'interface siliciure/Si est dans ce cas relativement plane. C'est dans cet intervalle de températures de recuit que l'on obtient, pour les films de siliciure avec ou sans oxyde interfacial, des conditions cristallographiques et morphologiques qui leur permettent de présenter les propriétés de transport les meilleures.

Les films de siliciure avec oxyde natif interfacial présentent la formation d'une couche continue de Pt_2Si en haut de la couche de siliciure, qui est déjà observable à 350 °C et qui reste inchangée même à haute température de recuit. L'existence de cette couche de Pt_2Si assure la continuité du film de siliciure jusqu'à 700 °C, même si les grains de PtSi au-dessous d'elle sont déjà épitaxiaux et isolés les uns des autres. Pour les échantillons sans oxyde, cette couche n'existe pas et la formations d'îlots est déjà observable entre 550 et 600 °C. La formation d'îlots mène à la discontinuité du film. La présence de la couche de Pt_2Si est donc bénéfique et même souhaitable pour préserver les propriétés de transport.

Quelques nanomètres de dégât d'irradiation sur la surface du substrat sont bénéfiques pour les couches ultra-minces de siliciure (3-5 nm). Les dégâts d'irradiation contribuent à ralentir le début de la formation d'îlots et augmentent l'intervalle de températures dans lequel les films gardent leur continuité et leurs propriétés de transport. Les dégâts d'irradiation peuvent augmenter légèrement la résistivité des films d'une épaisseur de 4-5 nm. Par contre des dégâts d'irradiation modérés, c'est à dire dans la gamme de profondeur susmentionnée, peuvent aider les films plus minces que 3.5 nm a améliorer leurs propriétés de transport, en leurs permettant d'atteindre des valeurs de résistivité plus basses qu'en absence de dégâts.

RESUMO

Os filmes finos de siliceto de platina são largamente usados em dispositivos de silício como contatos ôhmico e Schottky. Têm-se demonstrado recentemente que barreiras Schottky empregando filmes ultra-finos de siliceto de platina (espessura < 10 nm) podem ser usados em fotodetecção no infravermelho próximo.

Neste trabalho foi estudada a formação de filmes finos de siliceto de platina e suas propriedades elétricas em função da temperatura de recozimento. A influência de duas condições diferentes de preparação foram analisadas, isto é, estudou-se filmes de siliceto de platina obtidos por reação no estado sólido: a) em presença de uma camada interfacial de óxido de silício nativo de espessura variável; b) sobre substratos de silício que sofreram danos de irradiação em superfície, com profundidades variáveis, devido a uma limpeza adicional com bombardeamento por plasma. O interesse na investigação da influência dessas duas imperfeições do processo de limpeza da superfície do substrato sobre a reação Pt-Si e sobre as características estruturais e elétricas dos filmes de siliceto de platina é de origem tecnológica: tanto uma como outra ocorrem frequentemente na rotina de fabricação de tais filmes. Apesar de ser um evento frequente, até nossos dias, contraditoriamente, muito pouco foi relatado a respeito na literatura.

A qualidade e a reprodutibilidade dos films de siliceto de platina em fabricação rotineira depende fortemente do controle do processo, onde a limpeza do substrato desempenha um papel fundamental. O óxido de silício nativo pode estar presente devido a uma remoção incompleta por ataque químico antes da deposição do metal ou devido a um rápido recrescimento da camada de óxido após ataque químico. Sabe-se que uma camada de óxido interfacial pode causar problemas na metalização no contato de platina, embora as características resultantes dos filmes de siliceto de platina obtidos em função da espessura do óxido interfacial e da temperature de recozimento não sejam bem conhecidas. Por outro lado, para garantir a remoção completa da camada de óxido nativo, principalmente durante o delicado processo de fabricação de filmes ultra-finos de siliceto, um bombardeamento por plasma é aplicado sobre a superfície do substrato antes da deposição do metal. Este procedimento pode introduzir uma certa quantidade de danos na superfície do substrato que, por sua vez, podem influenciar a reação Pt-Si bem como a morfologia, cristalografia e características elétricas dos filmes obtidos.

As amostras foram preparadas usando-se diferentes ataques químicos e procedimentos para obter-se a remoção completa e incompleta do óxido nativo. O ataque por plasma na superfície do substrato foi aplicado com duração e potência de descarga variáveis a fim de obter diferentes profundidades de danos de irradiação por plasma. A reação de silicidação foi executada em temperaturas de recozimento diferentes. Cinco técnicas de caracterização foram empregadas para estudar essas amostras: Microscopia Eletrônica de Transmissão (TEM), Microscopia Eletrônica de Varredura (SEM), Microscopia de Fotoelétrons (PEM), Fotoemissão Interna (IPE) e Medidas por Quatro-Pontas. Das tres primeiras técnicas foram obtidas informações de caráter morfológico, composicional,

estrutural e cristalográfico, que foram subsequentemente correlacionadas com as propriedades elétricas dos filmes, obtidas através das duas últimas técnicas.

Observamos que os filmes de siliceto com camada de óxido interfacial de espessura de até 2.2 nm, recozidos em temperaturas apropriadas, são equivalentes aos filmes produzidos sobre substrato sem óxido no que conceme às aplicações práticas de metalização de dispositivos. As medidas de resistividade indicam o mesmo valor mínimo, 30 $\mu\Omega$cm, para os filmes com e sem óxido nativo interfacial, recozidos entre 350 e 550 °C.

O papel representado pela camada de óxido interfacial é preponderante durante as etapas preliminares da reação Pt-Si. Na ausência do óxido interfacial, o siliceto de platina é formado facilmente mesmo a baixas temperaturas ($T < 200$ °C). Em presença do óxido interfacial, a difusão dos reagentes se processa através dos poros do óxido nativo. Neste caso, a taxa de reação entre Pt e Si e a formação das fases de siliceto dependem principalmente da densidade e do diâmetro dos poros. Na faixa de temperatura de recozimento entre 350 e 550 °C, os filmes de siliceto obtidos com e sem óxido nativo interfacial alcançam uma estrutura estável, homogenea e bastante semelhante entre eles, consistindo de grãos policristalinos e epitaxiais de PtSi e uma interface siliceto/silício plana. Esta região de temperaturas de recozimento permite aos filmes de siliceto com e sem camada de óxido interfacial de alcançar condições morfológicas e cristalográficas que darão ótimas propriedades de transporte.

Os filmes produzidos em presença de camada de óxido interfacial apresentam, no entanto, uma particularidade: a existência de uma sub-camada contínua de Pt_2Si no topo da camada de siliceto, que se mantém inalterada mesmo sob recozimento a temperaturas mais altas. A existência desta sub-camada pode garantir a continuidade do filme de siliceto até 700 °C mesmo se os grãos de PtSi abaixo dela já são epitaxiais e isolados uns dos outros. Em amostras sem óxido interfacial a sub-camada de Pt_2Si não existe e a transformação para um filme do tipo 'ilha' é observada após recozimentos a temperaturas mais baixas (550 - 600 °C). A presença dda sub-camada de Pt_2Si é, portanto, benéfica e até mesmo desejável para melhorar as propriedades de transporte.

Alguns nanômetros de danos de irradiação por ataque de plasma na superfície do substrato são benéficos aos filmes ultra-finos (3 - 5 nm) de siliceto de platina. Os danos por plasma contribuem para retardar o início da formação de ilhas e estendem a faixa de temperatura de recozimento na qual os filmes de siliceto de platina mantêm a continuidade e as propriedades de transporte. Em filmes de siliceto com espessura entre 4 - 5 nm os danos por plasma podem aumentar ligeiramente a resistividade. Por outro lado, danos por plasma de profundidade de alguns nanômetros podem ajudar os filmes mais finos do que 3.5 nm a melhorar as propriedades de transporte.

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CHAPTER I

Introduction

Platinum silicide films are widely used in silicon devices, e.g., for ohmic and Schottky contacts [Murarka 1982]. In practical fabrication processes the chemical etching employed to remove the native silicon oxide from the Si substrate surface prior to metal deposition is often incomplete. An oxide film can be also present due to the fast native silicon oxide layer re-growth [Tu and Mayer 1978]. Then, an interfacial oxide film remains during Pt-Si reaction and may act as barrier to the atomic mobility. Up to now, it was not clear if a continuous and homogeneous silicide film can be produced in this situation. Some authors [Tu and Mayer 1978] alert to problems that this interfacial layer can cause to the contact metallization and establish a thickness range, 1.5 to 5.0 nm, as thickness that Pt can readily penetrate to form the silicide layer. Other authors [Liehr 1985] consider the possibility of Pt or Si migration through the pinholes if the native silicon oxide layer covers the Si surface completely (2.0 nm as maximum oxide thickness) preventing the direct contact between Pt and Si. However, questions as: *What is the role of the native oxide layer during the Pt-Si reaction? What kind of silicide film is obtained? What is the degree of crystallographic order expected for a silicide film produced in such conditions?* had no final response up to now. Furthermore, the electrical characteristics of such films as a function of the annealing temperature are unknown.

Ultra-thin films (thickness < 10 nm) are useful for photodetection [Sze 1981]. They are very important in the current silicide technology as semitransparent Schottky barriers for photovoltaic cells and infrared detectors. Platinum silicide films are particularly interesting as infrared image sensor in thermal imaging cameras [McCoy

1995]. The thickness range of these films makes their fabrication processes particularly delicate and a full contact between Pt and Si is fundamental to obtain good and re producible films. Because of this a complementary cleaning step, namely plasma etching bombardment, is used to guarantee the removal of all native oxide. However, the plasma etching bombardment can introduce a certain amount of damage in the substrate surface [Kondo 1992] which influence on the Pt-Si reaction as well as on the morphology, crystallography and electrical characteristics of these films is not well known up to now.

The aim of this work is to study the formation and properties of silicide films under the influence of these two imperfections due to the cleaning process on the Si substrate and establish the silicide preparation conditions to obtain the best transport properties. The Pt-Si reaction has been studied in the process conditions mentioned above, i.e., with an interfacial oxide layer or with a plasma etching damage on the substrate. Analyses of the morphological and crystallographic evolution as functions of the annealing temperature have been correlated with electrical characteristics obtained for these silicide films. The technological motivation is to improve electrical film properties and device reliability.

This work is organized as follows:

- In the present Chapter, we present a review of important results obtained for thin silicide films of interest to this work.

- In Chapter II, a brief overview of the platinum silicide formation and the expected crystallographic phases, as a function of the annealing temperature, is presented. We describe in detail our experimental procedure to clean Si substrates, to deposit metallic films and to anneal these films to obtain platinum silicide layers in the aimed conditions.

- In Chapter III, we present the characterization techniques used in this work describing the specific analysis conditions used for thin and ultrathin films.

- In Chapter IV, the results of the Pt-Si reaction with and without an interfacial oxide layer as a function of the annealing temperature are presented. The morphological and crystallographic evolution for the films obtained is analyzed in the 165 - 800 °C temperature range.

- In Chapter V, the results from resistivity measurements as a function of the annealing temperature are correlated to the morphological and crystallographic evolution of Pt-silicide films with an interfacial oxide layer and for Pt-silicide ultrathin films with plasma etching substrate damage.

- and finally, in Chapter VI, we present the conclusions obtained from our results and we propose process conditions to obtain continuous silicide films annealed up to temperatures as high as 700 °C and with better electrical properties than we can obtain with standard preparation conditions.

I.1 Thin silicide films for technological applications

Silicides: An Overview

The very large scale integration technology (VLSI) resulted in smaller and faster devices. In the early days one metal and one process were used. At present the complexity of integrated circuits and the increasing performance requirements of the devices necessitate multilevel metallization schemes and well-controlled heat treatments [Murarka 1983]. Higher packing densities and the increasing devices complexity renewed the interest in gates, interconnections and low resistance ohmic contacts. Therefore, new metallization processes became the subject of many studies in recent years.

The smaller the circuit, the more critical the interconnection resistance is. In 0.1 - 0.2 μm circuits, the delay due to the resistance (R) and capacitance (C) of the interconnection lines can be larger than those due to gate changes. The larger the product RC , the higher the probability that the circuit operation speed is limited by this delay. Thus, low resistance interconnections are very important to the high packing density and high performance circuits [Murarka 1983].

On the other hand, Schottky barriers can be used as fast and efficient photodetectors if the incident light is coupled into the depletion layer of the diode and if electron-hole pairs are created by the internal photoelectric effect in the depletion layer [Schneider 1966]. Fast response of the diode is achieved by designing a Schottky barrier with a small RC product.

Metal-silicon compounds, namely silicides, are particularly interesting for the technological applications mentioned above due to their low resistance and high temperature stability. They have been studied since the beginning of this century, when Moissan systematically prepared the first silicides [Moissan 1904], and are very useful for the recent microcircuits technology.

There are two broad classes of metal-silicon reaction products: eutectics and compounds (silicides) [Tu and Mayer 1978]. The Al-Si eutectic is one of the most widely used especially for interconnects. The major limitation on Al contacts to a semiconductors is the finite solid solubility of the silicon in aluminum which promotes the formation of pits on the silicon during the heat treatment. Silicide systems have the advantage of interacting with the semiconductor more uniformly than aluminum does. Silicide formation at low temperatures (~ 1/2 lowest eutectic) by the reaction between a metallic film and silicon leads to low-resistance contacts, and to the most reliable and reproducible Schottky barriers, with barrier heights ranging from 0.55 eV for $ZrSi_2$ to 0.94 eV for $IrSi_3$ on n-type Si. Furthermore, silicide usefulness is also due to the fact that they are ease to formed and stable during microcircuit processing and device use.

The choice of the silicide type and of its processing is a crucial technological point in using it as contact and gate in microelectronics. Crystallographical, morphological,

mechanical and electrical characteristics must be considered for each specific application.

Many elements of the periodic table, including rare earth and some simple metals, are able to react with Si and form one or more silicides. Silicides formed by metals from groups IVA, VA and VIA of the periodic table (called refractory metal silicides) and from group VIII (near-noble and noble metal silicides) are particularly interesting for the technological applications mentioned above. Table I.1 compare some characteristics of these two groups:

Property	**Group VIII**	**Group IVA, VA, VIA**
Resistivity of the metal	nearly the same for all metals: 7.5 ± 2.5 μΩcm	Decreases with atomic number in a period and in a group
Resistivity of the silicide	Nearly the same: 25 ± 10 μΩcm	Increases with atomic number in a period, and in a group
Crystal structure of the silicide	No correlation with the atomic number of the forming metal	The same for metals from the same group
Schottky barrier height (n-type Si)	Greater than half of the Si band gap energy; increases with the atomic number	All of them show similar values: 0.55± 0.05 eV
Formation temperature	200 - 600 °C	> 600 °C
Dominant diffuser	Metal	Silicon
High temperature stability (T > 1000 °C)	Poor	Good

Table I.1 - Characteristics of Noble and Refractory Metal Silicides (from S.P. Murarka, Silicides for VLSI Applications [Murarka 1983]).

I.2 Thin silicide films for ohmic contacts

The metallization in integrated circuits requires very low-resistivity contacts. This requirement is satisfied either by refractory or by near-noble metal silicides. As we saw in the previous section, near-noble metal silicides have nearly the same low resistivity at room temperature. Among them platinum silicide is probably the most generally used material as contact in integrated circuits [Tu and Mayer 1978], due to its usefulness in forming near-ideal ohmic (and also Schottky, as we will see later) contacts to both n- and p-type Si.

Resistance measurements with increasing temperature show that all silicides behave like metals: the resistance increases with the increasing temperature. However, sheet resistance values (R_s) measured at room temperature for one silicide formed at different annealing temperature can be very different. Furthermore, silicides formed by metals from the same metal group can show different sheet resistance evolution as a function of the annealing temperature. Murarka et al. [Murarka 1982] plotted the sheet resistance R_s ($\Omega/\square$) as a function of the annealing temperature in the 20 - 900 °C range for various silicides with different film thicknesses. We show this plot in Fig. I.1.

Three of them are near-noble metal silicides and all of them show a different resistance evolution with increasing annealing temperature. In particular, for platinum silicide films, the sheet resistance evolution is not surprising: authors found decreasing R_s values for platinum silicide films up to 400 °C, followed by constant values up to 850 °C and increasing R_s above this temperature. They attribute the high-sheet resistance values above 850 °C to the film discontinuity or preferred directional growth, due to the low temperature eutectic formation, observed by SEM.

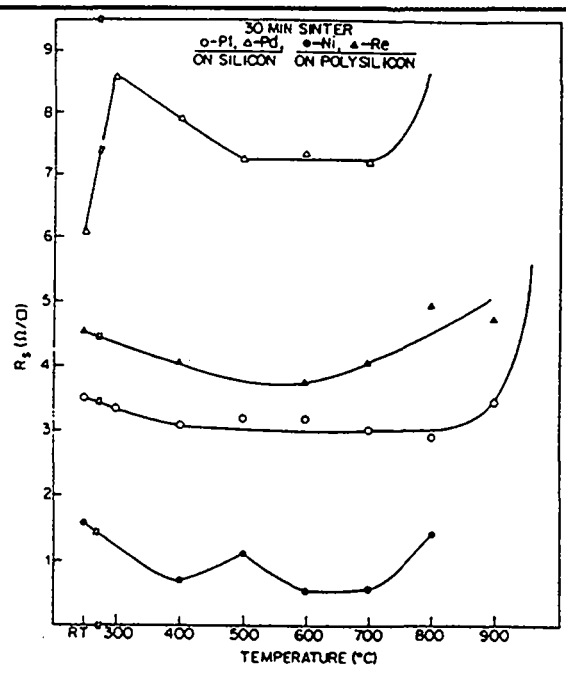


Fig. I.1: Sheet resistance (R_s) measured at room temperature as a function of the annealing temperature for 30 nm-thick Pd, 100 nm-thick Re, 50 nm-thick Pt and 170 nm-thick Ni silicides (from [Murarka 1982]).

I.3 Thin silicide films for Schottky contacts

In recent years, many works have led to several suggested mechanisms as being potentially responsible for controlling Schottky barrier heights, but no unifying mechanism has been established for the ensemble of silicide systems. We know, however, the evolution of the silicide Schottky barrier height as a function of several parameters, as binding energy [Grunthaner 1983], eutectic temperature [Ottaviani 1980] and Miedema electronegativity [Schmid 1985]. All this information was technologically important at its time and helps to form the present knowledgment in this domain.

Andrews and Phillips [Andrews 1975] proposed in 1975 a correlation between the Schottky-barrier height (ϕ_B) of transition metal silicides/Si and the heats of formation (ΔH_f). They successfully showed a simple linear relation (except for PtSi) between ϕ_B and ΔH_f : $\phi_B = 0.83 + 0.18\Delta H_f$. Later, when more measured data became

available ([Sze 1981]; [Murarka 1980]) and some values of ΔH_f were revised [Murarka 1982a], the ϕ_B - ΔH_f correlation lost part of its validity.

An interesting correlation between ϕ_B and the eutectic temperature was found by Ottaviani et al. [Ottaviani 1980] for transition metal silicide systems. They discovered that Schottky barrier height values decrease linearly with the eutectic temperature, where IrSi, PtSi and Pt_2Si exhibited the highest Schottky barriers (0.85 - 0.91 eV) and the lowest eutectic temperatures (1000 - 1100 °C); $ZrSi_2$ and TiSi present the lowest Schottky barriers (0.5 - 0.54 eV) and the highest eutectic temperatures (1650 - 1750 °C). In this correlation some anomalies present in the Andrews-Phillips work were removed, in particular those arising from 5d-noble metals silicide. However, the eutectic temperature is a parameter that involves many thermodynamic variables in a complex way and the theoretical background remained obscure.

Using the Schottky barrier values mentioned above, Grunthaner et al. [Grunthaner 1983], found that ϕ_B correlated with the strength of the transition-metals-Si orbital interaction as well as the charge density around the Si atoms for Ni, Pd and Pt silicides by XPS measurements.

Schmid [Schmid 1985], on the other hand, showed that there was a definite correlation between Miedema's electronegativity and ϕ_B for the elemental transition metals. He explained the correlation by an interface bond model, where the interface Fermi level was pinned in the bonding states and the bonding states values were correlated with Miedema's electronegativity. This correlation is shown in the Fig.I.2. This is a very successful model, also when one takes into account the interface density of states due to variable lattice mismatch between silicon and its silicides as in the Ni_2Si and NiSi case. In 5d-noble systems, however, such as PtSi, IrSi, and $IrSi_3$, with a lattice mismatch near 10% or more, barrier heights are nevertheless higher than with any other metals and roughly independent of composition of silicides.

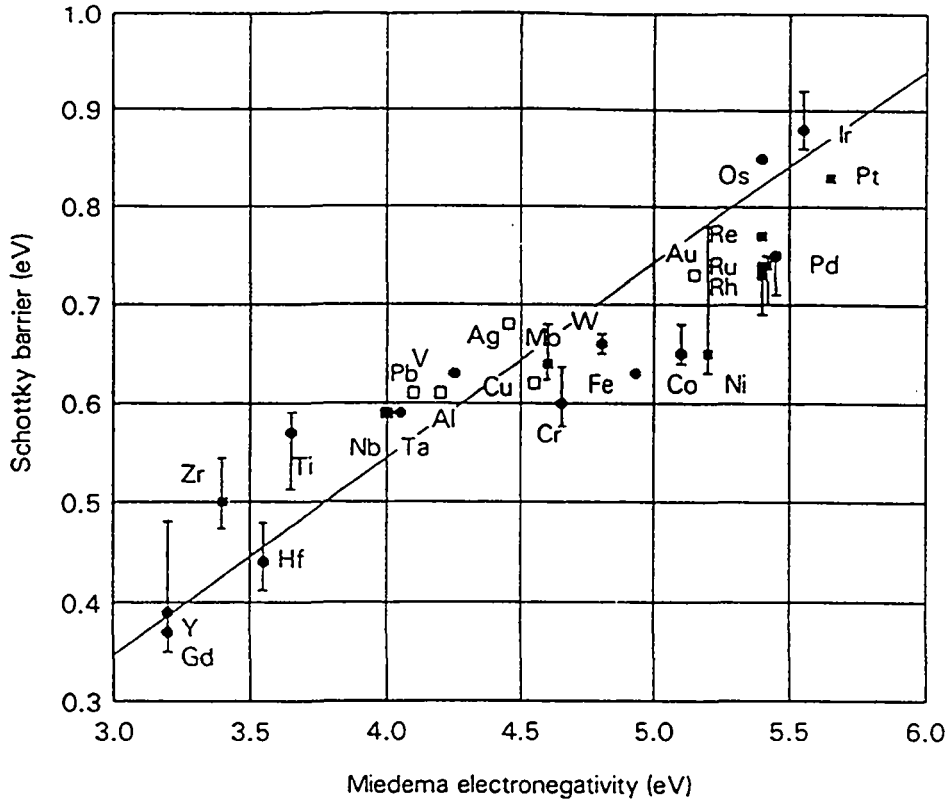


Fig. I.2: Barrier height of transition metal silicides and nonreacting metal Schottky barriers on n-type silicon. Solid circles and squares: silicides; open squares: nonreacting metals; solid circles: data from the literature (from [Schmid 1985])

I.4 Thin silicide films for photodetection

As we said previously, Schottky barriers can be used as a high-efficiency photodetector. This capability is strongly related to the current transport in a metal-semiconductor contact, which is mainly due to the majority carriers. A typical configuration of the current transport through an illuminated metal-semiconductor contact is shown in Fig. I.3 (from [Sze 1981]):

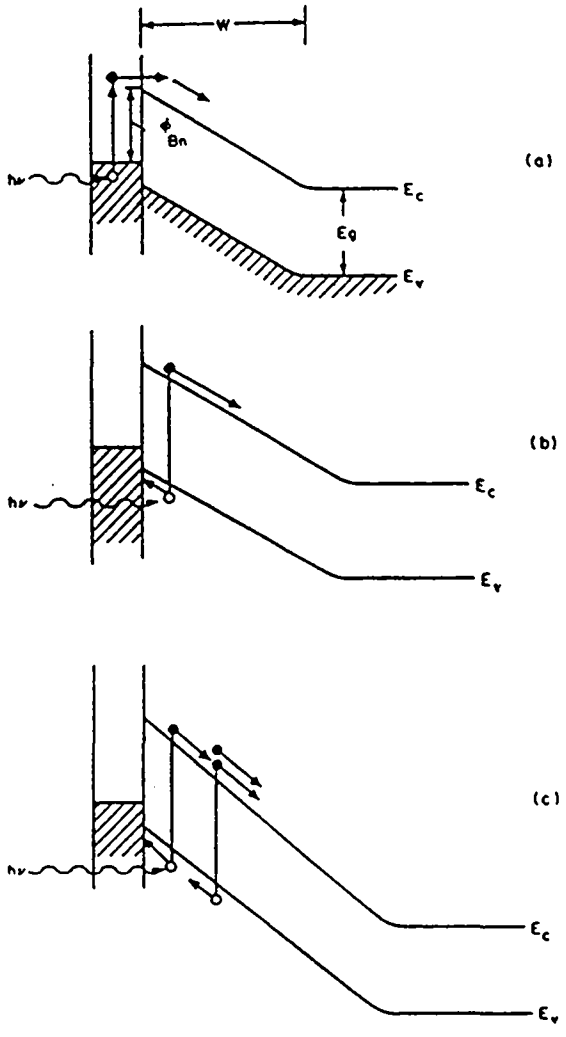


Fig. I.3: a) Photoelectron emission of excited electrons from metal to semiconductor ($E_g > h\nu > \phi_{Bn}$). **b)** Band-to band excitation of a hole-electron pair ($h\nu > E_g$). **c)** Hole-electron pair generation and avalanche multiplication under a large reverse bias ($h\nu > E_g$ and $V \cong V_B$) (from [Sze 1981]).

As shown in Fig. I.3, the diode can be operated in various modes, depending on the photon energy and biasing conditions:

1) For $E_g > h\nu > \phi_{Bn}$ and $V < V_B$ (Fig. I.3a), where V_B is the avalanche breakdown voltage, the photoexcited electrons in the metal can surmount the barrier and be collected by the semiconductor. This process has been used extensively to determine the Schottky-barrier height.

2) For $h\nu > E_g$ and $V < V_B$ (Fig. I.3b), the radiation produces hole-electron pairs in the semiconductor, and the general characteristics of the diode are very similar to those of a *p-i-n* photodiode.

3) For $h\nu > E_g$ and $V = V_B$ (high reverse-bias voltage) (Fig. I.3c), the diode can be operate as an avalanche photodiode.

Metal-semiconductor photodiodes are particularly useful in the visible and ultra-violet regions. Platinum silicide are also successfully used in the near infrared [Kimata 1987]. In this case, the platinum silicide photodiode operates as the example in the fig. I.3a: incident photons have energy smaller than the silicon energy gap, but higher than the Schottky barrier. Carriers are created in the metallic film and cross the Schottky barrier being collected by the semiconductor. To avoid large reflection and absorption losses when the diode is illuminated through the metal contact, the metallic film must be very thin (~ 10 nm) and an anti-reflection coating must be used. To be an efficient photodetector some requirements concerning the metallic film thickness have to be satisfied. We explain them below:

Small film thicknesses are necessary in photodetection to obtain high photocurrent yield. We can establish 10 nm as the appropriate thickness based on two different requirements:

1) to be a good photodetector, the film has to be opaque to the light. In other words, to generate electrons, at least 90% of the incident photons have to be absorbed in the film thickness to generate electrons. Losses are due to photons that cross the Schottky barrier and are absorbed in the semiconductor. The light absorption in materials is proportional to $e^{-\alpha r}$, where α is the absorption coefficient of light in the material and r the distance from the material surface. The absorption coefficient of light in materials, α, is defined as: $\alpha = 2\omega k/c$, where k the complex term of the refraction index, i. e., the coefficient of extinction [Wotter 1972]. The absorption coefficient α is ~ 10^6 cm^{-1} in metals, corresponding to an effective absorption length

of $1/\alpha \sim 10$ nm. Thus, this gives us the first requirement for the silicide film thickness d that has to be greater than $1/\alpha \approx 10$ nm.

2) In order to cross the Schottky barrier, the energy of carriers generated in the metallic layer have to be $E > \phi_{Bn}$ ($E \sim eV$). Losses in the energy of carriers have to be minimized on the path between the generation point and the barrier. Energy losses increase with increasing path due to carrier collisions. Under ideal conditions carriers should be generated in a film region whose distance to the semiconductor corresponds to the mean-free path of an electron, a quantity which is material dependent. Generally, the mean-free path falls in the 1 - 10 nm region, and this establishes the second condition to the choice of the film thickness d, $d \leq \lambda \leq 10$ nm, λ being the electron mean-free path.

From these two conditions we can estimate the ideal film thickness: $5 \leq d \leq 10$ nm.

REFERENCES

[Andrews 1975] J.M. Andrews and J.C. Phillips, Phys. Rev. Lett. **35**(1), 56 (1975).

[Grunthaner 1983] P.J. Grunthaner, F.J. Grunthaner and A. Madhukar, Physica B+C **117&118B**, 831 (1983).

[Kimata 1987] M. Kimata, M. Denda, N. Iwade, N. Tsubouchi, M. Daido, H. Furukawa, R. Tsunoda and T. Kanno, Optical Engineering, **26**(3), 209 (1987).

[Kondo 1992] I. Kondo, T. Yoneyama, K. Kondo, O.Takenaka and A. Kinbara, J. Vac. Sci. Technol. A **10**(5), 3166 (1992).

[Liehr 1985] M. Liehr, F.K. LeGoues, G.W. Rubloff and P.S. Ho, J. Vac. Sci. Technol. **A3**(3), 983 (1985).

[McCoy 1995] J.R. McCoy, Laser Focus World, p. 67 (July 1995).

[Moissan 1904] H. Moissan, "The Electric Furnace", Edward Arnold, London (1904).

[Murarka 1980] S.P. Murarka, J. Vac. Sci. Technol. **17**, 775 (1980).

[Murarka 1982] See, for example, S.P. Murarka, J. Vac. Sci. Technol. **B2**, 693 (1982).

[Murarka 1982a] S.P. Murarka, Mat. Lett. **1**, 26 (1982).

[Murarka 1983] S.P.Murarka, "Silicides for VLSI Applications", Academic Press, (1983).

[Ottaviani 1980] G. Ottaviani, K.N. Tu and J.W. Mayer, Phys. Rev. Lett. **44**(4), 284 (1980).

[Schmid 1985] P.E. Schmid, Helv. Phys. Acta, **58**, 371 (1985).

[Schneider 1966] M.V. Schneider, Bell Syst. Technol. J. **45**, 1611 (1966).

[Sze 1981] S.M. Sze, "Physics of Semiconductor Devices", 2nd edition, Wiley Interscience (1981).

[Tu and Mayer 1978] K.N. Tu and J.M. Mayer in "Thin Films - Interdiffusion and Reaction", edited by J.M. Poate, K.N. Tu and J.W. Mayer, Wiley Interscience, New York (1978).

[Wotter 1972] F. Wotter, "Optical Properties of Solids", Academic Press, New York (1972).

CHAPTER II

Sample Preparation

In this Chapter we describe the methods used to prepare our samples. The Si substrate cleaning, the metallic film deposition and the thermal reaction between the metallic film and the substrate are the main steps in the specimen obtainment. By varying systematically several processing parameters, we plan to study their influence on the silicide films.

To obtain good and reproducible platinum silicide films in routine fabrication, the process must be well-controlled. The silicide/silicon interface plays a crucial role in this process, thus much attention is normally devoted to the substrate surface cleanliness [Anderson 1975]. For example, for metals without or very little oxygen affinity (e.g., Pt, Co, Ni, Pd), the intermetallic formation can be retarded or even completely inhibited by a thin interfacial oxide layer between the silicon and the metal [Murarka 1983]. The use of conventional chemical etching procedures can result in an incomplete removal of the native silicon oxide layer. It is well known [Tu and Mayer 1978] that the native oxide layer can cause problems for Pt- or Pd-contact metallization if its thickness exceeds 5 nm. Thus, to ensure the complete cleanliness of the substrate surface, plasma etching before metallic deposition is a common procedure, in addition to the chemical etching [Anderson 1975]. However, plasma etching causes damage at the substrate surface. The influence of this damage, as well as that of native oxide layer on the subsequent Pt-Si reaction, is not well known. Thus, to obtain samples that will allow us to study the influence of these two imperfections due to the cleaning process in the final silicide film (Chapters IV, V and VI), we adopted the preparation procedures described below. Different chemical etching procedures were used to obtain complete and incomplete native oxide layer removal. Plasma etching on the substrate surface was also performed in a range of

discharge power to obtain different plasma etching damage depth. The silicidation reaction was performed at different annealing temperatures.

II.1 Si substrate etching

II.1.1 General

In order to study the influence of various substrate cleaning processes on the Pt-Si reaction and on the final characteristics of the silicide film, three different etching procedures were adopted. Two chemical etchings were used to obtain incomplete and complete native oxide removal; the third procedure, a combination between chemical etching and plasma etching, was used to obtain substrate surfaces free of silicon oxide.

The native silicon oxide film grows on a clean silicon surface in the first hours of exposition to an atmosphere containing oxygen (even at low partial pressure), and shows a tendency to saturation after ~ 16 hours, reaching a thickness of about 1.2 nm, as shown in Fig. II.1 (from [SD2200 ellipsometer PLASMOS catalogue]). The native SiO_2 growth was monitored by ellipsometry measurements. A re-growth of a 0.8 nm-thick silicon oxide layer during the first hour after cleaning is observed. Thus, a quarter of an hour is enough for the formation of a 0.2 or 0.3 nm-thick oxide layer, leading to changes in the Pt-Si reaction condition with respect to the oxide-free surface, as reported by Liehr et al. (1985) [Liehr 1985]. After a long oxygen-exposition time (several weeks), the SiO_2 layer thickness can even reach 5 nm.

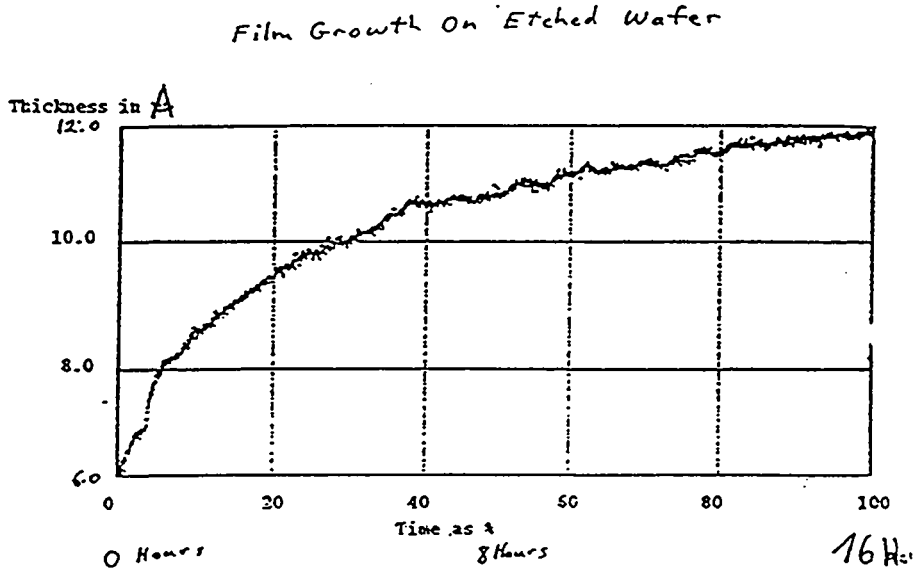


Fig. II.1: SiO_2 growth an etched wafer as a function of time (from: SD2200 Ellipsometer,PLASMOS Catalogue).

Several angstroms of the native oxide layer can also be present at this Si substrate surface due to an incomplete cleaning etch. Different chemical etch require different substrate dipping times, from 10 s (low pH aqueous HF solution) [Kern 1984] to several minutes (buffered HF, high pH) [Niwano 1994]. Furthermore, the etching rate depends on temperature. In routine procedures, we detect the native oxide removal by visual inspection: the substrate surface changes from a hydrophilic oxidized surface to a hydrophobic surface, which is a sign for a contaminant-free silicon surface [Kern 1984].

II.1.2 Incomplete native silicon oxide removal

In our work, the aim was to study the Pt-Si reaction with different interfacial silicon oxide layer thicknesses in the 1.5 - 5 nm range. According to Tu and Mayer [Tu and Mayer 1978], this is the oxide thickness range the metal atoms are able to penetrate to form the silicide layer. To obtain differences in oxide thickness, two methods could be used: an incomplete native silicon oxide etching or a native SiO_2 re-grown layer after an etching. The second method can require a long exposition time to produce different thickness larger than 1.5 nm. We preferred not to use the dry or wet thermal SiO_2 growth process, because the oxide layer grown by theses techniques does not have necessarily the same characteristics as the native oxide, e.g., uniformity and porosity ([Gibson 1980]; [Irene 1978]). Thus, we decided to adopt the incomplete native oxide etching method, with a rigorous control of reactant proportions and pH solution, and with only variations of the etching time.

In order to clean the substrate surface and to achieve a partial removal of the native silicon oxide layer, a two-step chemical procedure was employed. In the first step impurities such as organic residues were removed; in the second step, by using different etching time, different oxide layer thicknesses were obtained.

We used four-inch phosphorous-doped n-Cz (100)Si substrates with a resistivity of 3 - 5 Ωcm. Chemical solutions were prepared with pro analysi Merck products and bi-distilled water. The chemical procedure consists in removing organic impurities using successively hot trichloroethylene, acetone, methanol and isopropanol followed by substrate rinsing in de-ionized water. Immediately after that, some substrates were etched with buffered hydrofluoric acid (BHF) ($HF:NH_4F$, 1:10 in volume; pH: 5 - 6, at room temperature) for 5 seconds and other substrates for 15 seconds, to remove only part of the native oxide layer. The BHF was chosen because it is a mild and slow etch that allows a partial silicon oxide layer etching using reasonable etch times. Subsequently, wafers were rinsed in de-ionized water

for 5 minutes under ultrasonic agitation and under running de-ionized water. With this short BHF etching, the hydrophobic superficial state was not reached. Drying was performed using a nitrogen gas jet. The nitrogen used is a Carbagas product, with purity better than 99.999% and less than 2 ppm of O_2.

Following these procedures, we obtained two different thicknesses of native silicon oxide: (2.2 ± 0.3) nm, for substrates submitted to 5 seconds of BHF etching and (1.3 ± 0.2) nm for substrates having been dipped during 15 seconds in the same etch.

II.1.3 Oxide-free substrate surfaces

For complete removal of the native oxide, an HF:H_2O 1:200 in volume, pH: 1.5 - 2, chemical etching for 30 s was performed for another group of substrates. This etching is widely used to remove SiO_2. In choosing this etching we expect to obtain H-passivated Si(100) surface mostly covered with SiH_2 [Higashi 1990]. Some roughness is also expected, but less than when using buffered HF (pH ≈ 5.0) that increases the monohydrate (SiH) formation (ideal covering) but leads to a formation of Si(111) facets [Higashi 1990]. These authors also shown that the more basic the HF solution, the more anisotropic the treated surface. To minimize roughness, we chose an acid solution. Prior to the silicon oxide removal, organic impurities were removed by the procedure previously described. Also rinsing and drying procedures were performed as in the previous section. For all substrates, we found the evidence of the silicon oxide removal, i.e., the change of an hydrophilic oxidized surface to hydrophobic. After drying, some of these substrates received directly the metallic film by sputtering deposition and others were submitted to plasma etching prior to metallic film deposition.

Ar^+ plasma etching was performed in the sputtering chamber just before metallic deposition. The plasma discharge power and the bombardment time were varied to obtain different plasma etching damage depth. The pressure in the chamber was 5 x 10^{-3} mbar during plasma etching.

II.2 Metallic film deposition

For metal film deposition, a radio-frequency (RF) magnetron sputtering machine equipped with a mass spectrometer was used. The distance between the Pt target and the Si substrate was 80 mm. The total residual pressure in the chamber before deposition (due to partial pressures of H_2O, N_2 and CO) was 2 x 10^{-6} mbar. The argon pressure during the sputtering deposition was 7 x 10^{-3} mbar. We RF-sputtered :

a) (14 ± 0.5) nm-thick Pt films on (3 - 5 Ωcm) n-Cz Si(100) substrates with an interfacial silicon oxide layer (2.2 nm- and 1.3 nm-thick).

b) 12 nm- and 3 nm-thick Pt films on (3 - 5 Ωcm) n-Cz Si(100) substrates without interfacial silicon oxide and without plasma etching.

c) 3 - 5 nm-thick Pt films on (22 - 27 Ωcm) n-Cz Si(100) substrates without interfacial silicon oxide and with 50 or 100 W plasma etching during 2-7 minutes. The deposition time was varied slightly to obtain different metal layer thickness.

All substrates were heated to 165 °C for 30 minutes before metal deposition and kept at this temperature during the deposition process. This procedure allows to minimize the deposition defects in as-deposited films (before annealing) and improves adherence. The total pressure after deposition decreased to 6 x 10^{-7} mbar. After cooling to room temperature, the deposition chamber was slowly pressurized to the atmospheric pressure and samples were removed and placed immediately in a temperature-stabilized furnace for annealing. The substrate transport was made in a dessiccating apparatus under vacuum (~ 10^{-3} mbar). Chemical etching and metal deposition were performed in a clean-room.

II.3 Obtainment of platinum silicide films: solid-solid reaction

II.3.1 General

Many different phases can be obtained by annealing metal/Si at subeutectic temperatures. The phase diagram for platinum silicides is shown in Fig. II.2 [Massalski 1986]. The lowest eutectic point is 830 °C for the Pt_3Si phase. Two different structures are seen for Pt_2Si, the α-phase until 695 ± 5 °C and the β-phase, between 695 ± 5 and 986 ± 4 °C. The existence of the platinum monosilicide is allowed until 983 ± 5 °C.

The existence of the metal-rich phase $Pt_{12}Si_5$ is not mentioned in the phase diagram, although information about the two different $Pt_{12}Si_5$ tetragonal structures can be obtained in the literature ([Gold 1969]; [Ram 1978]).

The first model to predict the phase formation sequence was proposed by Walser and Bené [Walser 1976]. These authors found that the first crystalline phase nucleated is the congruently melting phase next to the lowest-temperature eutectic. A few years later, Tsaur et al. [Tsaur 1981] proposed a general model for the phase formation in metal-Si interactions based on the previous model proposed by Canali et al. (1979).

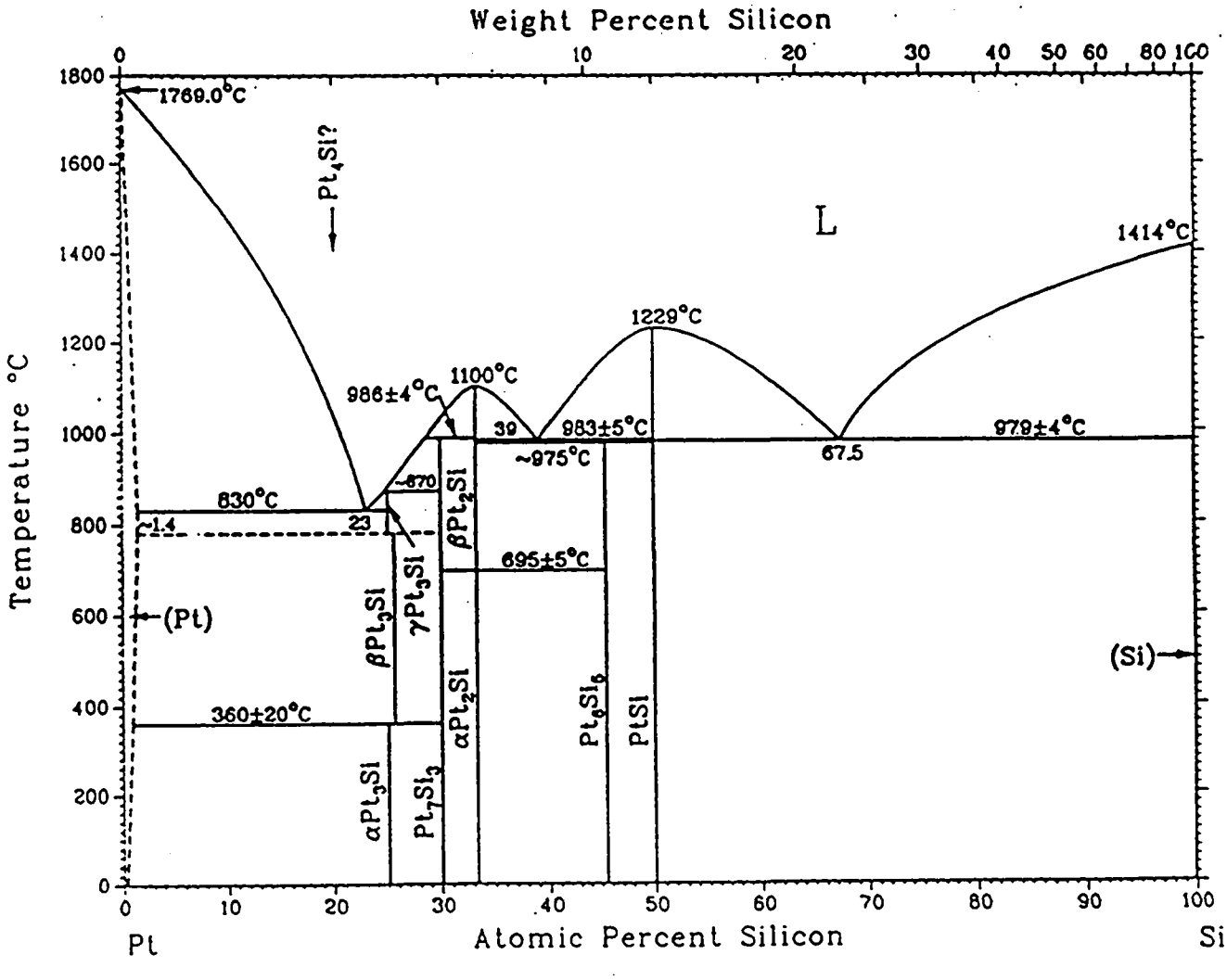


Fig. II.2: Pt - Si phase diagram (from: [Massalski 1986]).

Silicide phase	Structure	Space group	Lattice parameter
PtSi	Ortorhombic	Pbnm(62)	a = 0.5932 b = 0.5595 c = 0.3603 $\alpha = \beta = \gamma = 90°$
Pt_2Si	Tetragonal	I4/mmm (139)	a = b = 0.3933 c = 0.5910 $\alpha = \beta = \gamma = 90°$
Pt_3Si	Monoclinic	F2/m (12)	a = 0.7702 b = c = 0.7765 $\alpha = \gamma = 90°$ $\beta = 88.11°$
Pt_3Si	Ortorhombic	Pnma (62)	a = 0.5579 b = 0.7697 c= 0.5520 $\alpha = \beta = \gamma = 90°$
$Pt_{12}Si_5$	Tetragonal	P4/n (85)	a = b = 1.3404 c = 0.5451 $\alpha = \beta = \gamma = 90°$
$Pt_{12}Si_5$	Tetragonal	I4/m (87)	a = b = 0.9607 c = 0.5542 $\alpha = \beta = \gamma = 90°$

Table II.1: Platinum silicide phases found in the the phase diagram with their crystallographic structure and the space group to which they belong (source: Joint Commitee of Powder Diffraction Standars (JCPDS) cards: 7-251; 17-683; 17-670; 34-956; 22-782; 34-903).

The schematic diagram of phase formation proposed by Tsaur et al. [Tsaur 1981] is shown in the Fig. II.3. In the initial stage of the reaction the first phase: M_mSi_n ($m \neq n$ and M = metal) forms at the Si-metal interface. After one of the elements (Si or metal) has been consumed in the growth of the M_mSi_n, the reaction is driven toward

the phases that are richer in the remaining element. If the thickness of Si is much greater than that of metal, a second phase richer in Si ($M_{x<m}Si_n$) will generally start to form at the Si-M_mSi_n interface. Most of the experiments of this type were carried out with metal films deposited on single-crystal Si substrates [Tu and Mayer 1978]. On the other hand, if the thickness of the metal is much greater than that of Si, the next phase formed at the metal-M_mSi_n interface will be a more metal-rich silicide $M_{x>m}Si_n$. The experiments of this type are usually performed with metal films deposited on amorphous Si films or inert substrates [Canali 1979]. For Ni, Pd, Pt and Co, the previous models predict that the first phase formed is the metal-rich phase (in practically all cases this phase is M_2Si).

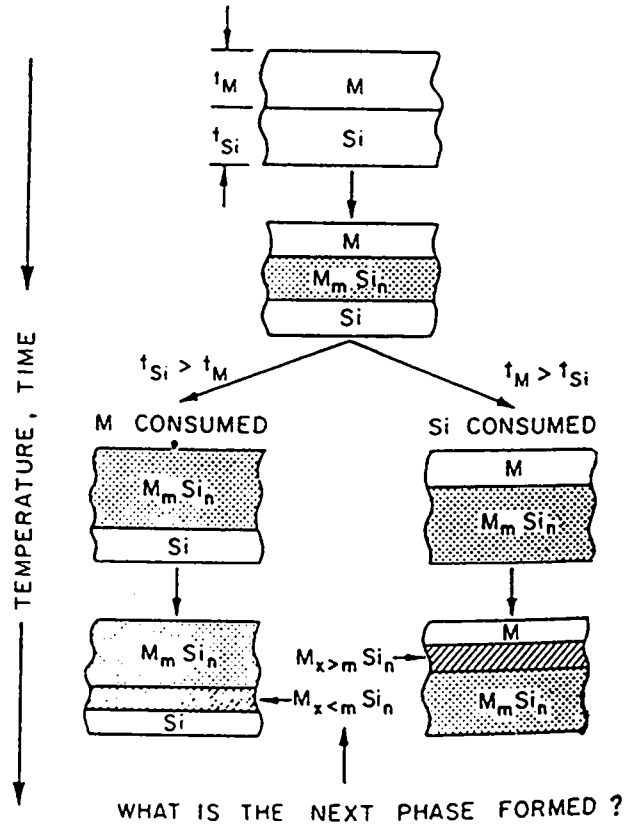


Fig. II.3: Schematic diagram showing the phase formation in metal-silicon interaction (from: [Tsaur 1981]).

Murarka et al. [Murarka 1982], at the same time, published experimental results on thin metal layers deposited on polysilicon confirming the predictions of the previous

models. For a (50 ± 2.5) nm-thick platinum silicide film, e.g., they detected Pt_2Si (the metal-rich phase) formation at 200 °C and PtSi between 300 and 900 °C.

Finally, in 1985, Majni et al. [Majni 1985] published a schematic diagram showing the sequence of phase formation in Pt - Si interaction. Silicides are no longer considered as 'alloys', as in the traditional nomenclature [Muta 1972] but as compounds. For the Pt-Si system, they found different sequences of phase formation with the increase of the temperature according to the relative quantity of Pt and Si atoms avalilable for reaction (Fig. II.4). Our samples, obtained by solid-solid reaction of a nanometric metallic film and a Si substrate (590 µm-thick) fall mostly in the first case showed in the diagram: much more Si than Pt atoms are available for reaction.

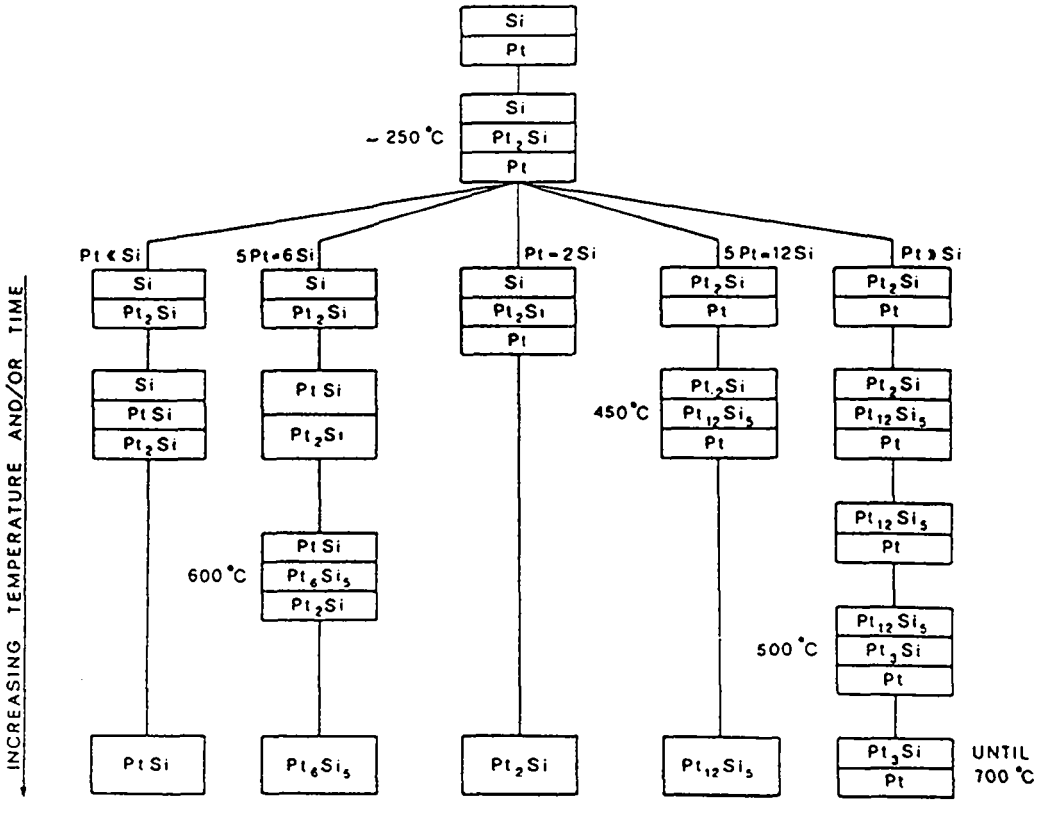


Fig. II.4: Schematic diagram showing the sequence of phases formation in the Pt-Si thin film interaction (from [Majni 1985]).

This case coincides with the phase formation predicted by the previously mentioned models, where the first phase formed is Pt_2Si. By increasing the temperature, Pt_2Si reacts with Si to form PtSi ($Pt_2Si + Si \rightarrow 2PtSi$), that is the final phase. Some exceptions to this phase formation sequence will be seen in Chapter IV, were another metal-rich phase ($Pt_{12}Si_5$) is observed simultaneously with Pt_2Si in our samples.

Silicide	Formation Temperature (C)	Activation energy of growth (eV)	Growth rate	Crystal structure	D_0 (10^{-2} cm^2/s)
Pt_2Si	200 ~ 500	1.1 ± 0.1 (MS) 1.6 ± 0.1 (PT) 1.3 ± 0.2 (CP)	$t^{1/2}$	Tetragonal	0.15 (MS) 890 (PT)
PtSi	≥ 300	on Si(111): 1.5 ± 0.1 (MS) on Si(111) and (100): 1.6 ± 0.1 (PT) on Si(100): 1.5 ± 0.2 (CP) on Si(111): 1.6 ± 0.10 (W) on Si(100): 1.45 ± 0.10 (W)	$t^{1/2}$	Ortorhombic	25 (MS) 63 (PT) 130 (W) 7.8 (W)

Table II.2 - Formation parameters for platinum metal-rich and monosilicide for n-doped substrates (from Tu and Mayer [Tu and Mayer 1978]; D_0 values have been published by Muta and Shinoda (MS) [Muta 1972]; Poate and Tisone (PT) [Poate 1974]; Crider and Poate (CP) [Crider 1981]: Wittmer (W) [Wittmer 1983].

For metal-rich silicides, the growth kinetics follows a square-root-of-time law and an activation energy around 1.5 eV. Monosilicide formation is also characterized by a

parabolic growth rate but with an activation energy between 1.6 and 2.5 eV. The formation temperature for monosilicides is higher than that for metal-rich silicides and generally occurs above 350 °C. Table II.2 summarizes the formation parameters of the metal-rich (Pt_2Si) silicide and the monosilicide (PtSi) of interest for this work.

The growth rate following a $t^{1/2}$ law means that the process is controlled by interdiffusion of Pt and Si, obeying equation 1 below [Poate 1974]; [Muta 1972]; [Kidson, 1961]:

$$d = 2D^{1/2} t^{1/2} \qquad \text{eq. 1}$$

where d is the layer thickness, t is the duration of the heat treatment and D is the chemical interdiffusion constant. $D(T)$ is given by:

$$D(T) = D_0 \exp(-E_a/kT) \qquad \text{eq. 2}$$

where E_a is the activation energy, D_0 an preexponential factor, k is Boltzmann's constant and T the absolute temperature. The table II.1 lists the values for the preexponential factor D_0, found by Muta and Shinoda and Poate and Tisone for Pt_2Si and PtSi on Si(111) and by Wittmer for PtSi on Si(100) and (111). Wittmer found that D_0 depends on substrate type and doping. For Pt_2Si, D_0 values obtained by Muta and Shinoda are in disagreement with those obtained by Poate and Tisone. The difference is due to the growth mechanism: simultaneous Pt_2Si and PtSi growth is observed by Muta and Shinoda, in contradiction with results from Poate and Tisone, who observed PtSi formation at the Pt_2Si/Si interface only after complete Pt_2Si formation. In Chapter IV we discuss both cases, as they are found in silicide films with and without interfacial oxide layer.

II.3.2 Experimental

The as-deposited wafers were cleaved in 2 x 2 cm squares. A square from each wafer was annealed to one of the following temperatures: 180, 250, 350, 450, 500, 550, 600, 650, 700, 750 and 800 °C (in way that one square was annealed to one and only one temperature) for 30 minutes in a conventional furnace under ultra-pure argon. 800 °C was chosen as the highest annealing temperature because it is just below the lowest Pt-Si binary eutectic point, 830 °C , for the Pt_3Si phase.

We used a one-zone furnace, equipped with a PID 810-type Eurotherm control. This allows a thermal stability better than 5% during the furnace cycle. Prior to annealing, a baking is performed at 800 °C and the furnace is evacuated to 2 x 10^{-2} mbar with an oil-free pumping system. During heat treatment a constant flow of 3.3 x 10^2 cc/min. of Ar was maintained (purity > 99.9997%, O_2 < 0.3 ppm). The temperature ramp, after sample introduction, was 80 degrees/min. The annealing time was considered from the moment at which a stable temperature was reached. After 30 minutes, we cooled samples at 60 degrees/min.

REFERENCES

[Anderson 1975] R.M. Anderson and T.M. Reith, J. Electrochem. Soc., **122**(10), 1337, (1975).

[Canali 1979] C. Canali, G. Majni, G. Ottaviani and G. Celotti, J. Appl. Phys. **50**(1), 255 (1979).

[Crider 1981] C.A. Crider, J.M. Poate, J.E. Rowe and T.T. Sheng, J. Appl. Phys. **52**(4), 2860 (1981).

[Gibson 1980] J.M. Gibson and D.W. Dong, J. Electrochem. Soc. **127**(12), 2722 (1980).

[Gold 1969] Gold and Schubert, Z. Kristallogr. **128**, 406 (1969).

[Higashi 1990] G.S. Higashi, Y.J. Chabal, G.W. Trucks and K. Raghavachari, Appl. Phys. Lett. **56**(7), 656 (1990).

[Irene 1978] E.A. Irene, J. Electrochem. Soc. **125**(10), 1708 (1978).

[Kern 1984] W. Kern, Semicond. Intern. **7**, 94 (1984).

[Kidson 1961] G.V. Kidson, J.Nucl. Mater. **3**, 21 (1961).

[Liehr 1985] M. Liehr, F.K. LeGoues, G.W. Rubloff and P.S. Ho, J. Vac. Sci. Technol. **A3**(3), 983 (1985).

[Majni 1985] G. Majni, M. Costato, F. Panini and G. Celotti, J. Phys. Chem. Solids **46**(5), 631 (1985).

[Massalski 1986] T.B. Massalski in "Binary Alloy Phase Diagrams" - ed.-in-chief: Taddeus B. Massalski, ed.; 1st ed., p. 1909, American Society (1986).

[Murarka 1982] S.P. Murarka, M.H. Read, C.J. Doherty and D.B. Fraser, J. Electrochem. Soc. **129**(2), 293 (1982).

[Muta 1972] H. Muta and D. Shinoda, J. Appl. Phys. **43**(6), 2913, (1972).

[Niwano 1994] M. Niwano, J. Kageyama, K. Kinashi, N. Miyamoto and K. Honma, J. Vac. Sci. Technol. **A12**(2), 465 (1994).

[PLASMOS Catalogue] SD 2200 Ellipsometer, PLASMOS Catalogue, PLASMOS GmbH Prozeβtechnik. Measurements performed in cooperation with Fraunhofer Institute of Integrated Circuits (1980).

[Ram 1978] R. Ram and Z. Bhan, Z. Metallkd. **69**, 524 (1978).

[Tsaur 1981] B.Y. Tsaur, S.S. Lau, J.M. Mayer and M.-A. Nicolet, Appl. Phys. Lett. **38**(11), 922 (1981)

[Tu and Mayer 1978] K.N. Tu and J.M. Mayer in "Thin Films - Interdiffusion and Reaction", edited by J.M. Poate, K.N. Tu and J.W. Mayer, Wiley Interscience, New York (1978).

[Walser 1976] R.M. Walser and R.W. Bené, Appl. Phys. Lett. **28**(10), 624 (1976).

[Wittmer 1983] M. Wittmer, J. Appl. Phys. **54**(9), 5081 (1983).

CHAPTER III

Experimental Characterization Techniques

In this Chapter the five experimental techniques we used to characterize our platinum silicide samples are described. These techniques are: Transmission Electron Microscopy (in conventional (TEM), Electron Diffraction (ED) and High Resolution (HRTEM) modes), Scanning Electron Microscopy (SEM), Photoelectron Microscopy (PEM), Internal Photoemission (IPE) and Four-Point Probe Measurements. Morphological, compositional, structural and crystallographic information is obtained from the first three techniques. They reveal how the silicide film forms and develops as a function of the annealing temperature. This information is then correlated to the electrical properties of the films studied with the last two techniques.

Morphological information from the sample surface, without specimen thinning or metallic coating is obtained by high resolution SEM.
Phase transformations, changes in crystallographic order and morphology are observed by TEM. In particular, the analysis of HRTEM cross sectional images enabled us to establish the silicide phase distribution across film thickness and the crystallographic interface correlation between the silicide film and the substrate for every annealing temperature with resolution better than 0.20 nm.
The homogeneity of the specimen was examined over a large area with spatially resolved chemical information by PEM.

Internal Photoemission and Four-Point Probe measurements describe the behavior of Schottky barrier height and resistivity for different types of silicide films as a function of the annealing temperature. This correlation gives the annealing conditions which lead to the best platinum silicide transport properties.

III.1 Transmission electron microscopy (TEM)

III.1.1 Observation Conditions

The electron microscopy is one of the most useful characterization techniques in materials research. It is widely used in scientific and industrial investigations for developing either fundamental science or technology and its capabilities have been considerably increased in the last decades. Extensive reports on the operation of the electron microscope and the physics of the image formation have been published by several authors ([Reimer 1984]; [Spence 1981]; [Hirsch 1967]).

In order to investigate the Pt - Si reaction steps as a function of the annealing temperature we employed the Transmission Electron Microscopy (TEM) in three different observation modes: Conventional TEM, Electron Diffraction (ED) and High Resolution TEM. We used the Philips EM-430 ST microscope with a LaB_6 rod as a cathode, at an accelerating voltage of 300 kV for all TEM analyses.

In conventional transmission electron microscopy (TEM) we obtained low-magnification planar-view images in bright-field mode from silicide films. Observations were performed through the Si[100] direction, with the silicide film on top. The continuity (or island formation) and the texture of the silicide film over a large area are analyzed by means of these observations. Grain shape and size are measured on this kind of imaging. The presence of Moiré fringes was often detected for grains in annealed samples, allowing to evaluate, in a general view, the grain orientation with respect to the substrate: Moiré fringes result from a superposition of the grain crystalline lattice to that of the monocrystalline Si substrate. To increase the contrast, an objective aperture was used. We employed systematically a low magnification (59000 X) for an overview of the sample.

In high resolution mode (HRTEM) atomic planes or atomic columns (depending on imaging conditions and interplanar spacing) can be visualized as interference

fringes formed by the transmitted and diffracted beams, that reflect the crystalline periodicity. Detailed reports of general or specific electron scattering conditions can be found in the literature [e.g., Ishizuka 1980]. In this work, HRTEM images were obtained from cross-sectional samples showing the silicide film and the Si substrate. Observations were performed through the Si[110] direction, as the example shown in Fig. III.1. We were able to measure the thickness of sub-nanometric layers, as in the case of the interfacial oxide layer thickness in Chapter IV. The silicide phase distribution along the silicide film thickness was established and the flatness of the silicide/Si interface (up to atomic level) was evaluated. The EM-430 ST microscope was operated in high resolution mode, giving a resolution better than 0.20 nm and a 30 μm-diameter condenser aperture was employed in a systematic magnification of 700000 X at the appropriate defocus condition.

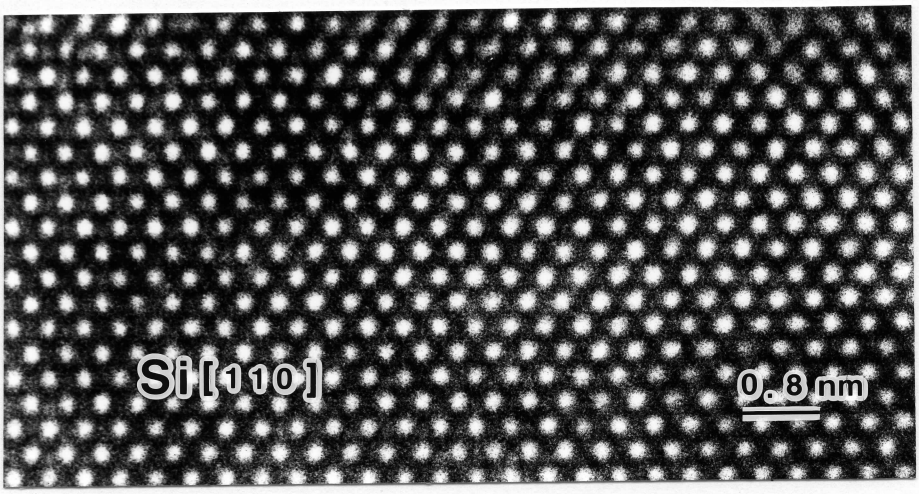


Fig. III.1 - Cross-sectional HRTEM image of a Si substrate, as used in our samples, observed in the [110] direction.

The electron diffraction and its interpretation as well as the physics related to diffraction patterns obtained with an electron microscope have been treated as specific subject by many authors ([Edington 1975]; [Vainshtein 1964]).

We obtained electron diffractograms from the same "planar view" preparations used for TEM observations. Electron Diffraction (ED) patterns come from the same area previously photographed in the bright-field mode. The patterns always contain the silicide film diffraction superimposed to that of the Si substrate in [100] direction. We list below the four basic ED patterns shown in Chapter IV and V for silicide films:

1) spot pattern (discrete reflections shaped as spots): obtained from single crystals or groups of single crystals (mosaics);

2) texture patterns (discrete spots distributed over rings or arc reflections): obtained from crystals uniformly oriented on the specimen substrate and having one degree of freedom (one face being parallel to the substrate but random azimuthal distribution of the crystals);

3) polycrystalline patterns (spots or arcs forming sharp and continuous ring reflections): obtained from aggregates of randomly-distributed crystals.

4) amorphous pattern (broad and continuous ring reflections): obtained from amorphous or quasi-amorphous material.

ED patterns can show the superposition of two or more types listed above with different degree of crystalline order. In Chapters IV and V, we discuss the case where different platinum silicide phases in different degree of order (epitaxial, mosaic textured and polycrystalline grains) are superposed to a well-known monocrystalline Si substrate. The Si pattern is taken as a reference to analyze the platinum silicide pattern. First, the Si spots taken in a specific Si zone axis are indexed, with the interplanar distance d for each of them. This gives us the camera length from which the (hkl) indices and the interplanar distance d for each platinum silicide atomic plane can be calculated. The comparison with tabulated values gives the silicide phase. In the spot pattern case, we also calculate the incident beam direction $\boldsymbol{B}$ ($\boldsymbol{B} = \mathbf{g}_1 \wedge \mathbf{g}_2$, where $\mathbf{g}_1$ and $\mathbf{g}_2$ are the vectors defined by ($h_1k_1l_1$) and ($h_2k_2l_2$)).

III.1.2 Sample preparation

Two types of sample preparation for TEM, planar-view and cross-section (see, for instance, [Hirsch 1967]; [Heimendahl 1980]), were performed for all annealed wafers.

In TEM planar-view observations, the electron beam crosses the whole thickness of the silicide film and the remaining Si substrate projecting on the screen a morphological view of the sample. For planar-view sample preparation, the PtSi layer side of a small piece of PtSi annealed film + Si substrate was glued to a copper ring and the backside of the Si substrate was mechanically polished. The sample was thinned to the electron transparency by ion milling, with a 5 KeV Ar^+ ion beam, bombarding only the backside of the silicon substrate. A cooling system using liquid nitrogen was employed for as-deposited or low temperature-annealed samples.

In our cross sectional images we can observe the whole film thickness, the interface silicide/silicon and part of the silicon substrate bulk. Cross section preparation procedure requires more steps than planar-view. First, two small bars of the same sample were glued together (with an epoxy glue as Araldite) on the silicide film side; this 'sandwich' was put in a cylinder holder and then slices were cut. Both sides of these slices were manually polished down to mirror smoothness (~ 30 μm-thick sample). The thinning was finished with a 5 KeV Ar^+ ion bombardment, on both sides. Low temperature-annealed samples were cooled down during bombardment.

III.1.3 Computational methods to interpret HRTEM images and ED patterns: the EMS program

EMS is a powerful software package developed by P. Stadelmann [Stadelmann 1987] for simulation and analysis of High-Resolution Electron Microscopy images and for the analysis of diffraction patterns. Typical crystallographic calculations to interpret electron microscopy information such as indexing of diffraction and Kikuchi patterns, simulation of spot and powder patterns, drawing of stereographic projections, calculation of Bravais lattice of an unknown structure from two diffraction patterns, etc. can be obtained. EMS software also allows to simulate structure images using a Fast-Fourier-Transform-based multislice approach or Bloch Waves.

III.2 Scanning Electron Microscopy (SEM)

We performed SEM analysis on our samples as preliminary characterization after annealing. The surface of the specimen was observed for evaluating the grain formation and superficial changes as a function of the annealing temperature. Morphological information obtained with SEM comes from the surface (or some nanometers below the surface).

As a high resolution was required in order to observe the nanometric grains of our samples, we performed our analysis with a high-resolution microscope equipped with a field emission gun, the JMS-6300F JEOL scanning microscope. It is able to provide high resolution performance and lower noise at low accelerating voltages and high quality secondary electron images. Its secondary electron image resolution is 1.5 nm at 30 KV and 8 mm-working distance. These are the best conditions to obtain the maximal resolution. Field emission guns are now used as electron sources instead of conventional electron guns because of their high brightness.

Our secondary-electron analyses were performed with a final energy beam of 10 KV, (resolution better than 2.0 nm), magnification of 50000 X, and tunable working distance (8 - 15 mm) and probe current (10^{-12} to 10^{-10} A). Samples were not metallized due to the possibility to observe them with good resolution at low voltages (5 kV). This kind of observation was performed even for samples with a discontinuous metallic film, where the beam interacts directly with the Si surface, as shown in Chapter V. They were fixed mechanically on the sample holder, without colloidal silver glue.

III. 3 Photoelectron microscopy

Analyses using Photoelectron Microscopy were performed in our samples in order to obtain simultaneous topographical and chemical information from large areas of the sample surface. The Photoelectron Microscope (PEM) is an emission microscope able to produce images of solid surfaces using the electrons emitted after photon absorption [Mollendstedt 1963]. Furthermore, it provides spatially resolved chemical information of sample surface by detecting and analyzing the kinetic energy of the outgoing photoelectrons.

Real-time images produced by photoelectrons have been obtained for our platinum silicide samples using synchrotron radiation, in the ultraviolet and soft x-ray regions. Energies in the range from 40 to 120 eV were used to produce images with lateral resolution of the order of some μm.

Monochromatic synchrotron radiation was produced by beamline U12 at the Synchrotron Radiation Center (SRC) at Madison, Wisconsin, USA. The U12 beamline is 3 meters long and uses a toroidal-grating monocromator for energies between 10 and 155 eV, with a focused spot of ~1 mm diameter. Due to mechanical constraints, the spot size of the incident photon beam on the sample (1 x 5 mm) was

not well matched to the image field-of view, which was typically 200-500 μm in diameter [Tonner 1989]. Spectra were obtained in the 40 - 60 eV range to detect *5p* electrons from Pt atoms and in the 98 - 112 eV range to detect *2p* electrons from Si atoms.

Our measurements were performed using the PEM microscope developed by B. Tonner and co-workers ([Tonner 1988]; [Tonner 1989]; [Tonner 1990]). Electrons emitted by the sample surface reach the single electrostatic lens and are imaged by it. The lens consists of an anode (A) and a focusing element (control electrode or Wehnelt). In the present configuration, the sample is biased to high potential (–8 to –10 keV), the anode is grounded and the control electrode potential is adjusted to focus at the image plane. A small aperture (≤ 100 μm-radius) is placed in the back focal plane of the objective lens to improve spatial resolution. The aperture also has the effect of providing some energy filtering of the image.

Image magnification can be changed by changing the lens polarization because the focal length (~ mm) is a direct function of the control electrode (Wehnelt) bias. The magnified image of the sample surface is intensity-amplified by a single microchannel plate (MCP) array and on phosphor screen assembly. The image formed on the phosphor screen is detected with a video camera outside the vacuum system. The camera tube is a silicon-diode-array tube (RCA 4532U) which is scanned by a frame grabber and stored in memory as a 512 x 512 pixel array of 8-bit depth. The use of monochromatic synchrotron radiation allows the enhancement of chemical contrast by digital subtraction of images formed with photon energies above and below absorption threshold of the corresponding chemical element.

For these measurements we used the same samples observed by SEM just cleaved in appropriate dimensions to be put onto the sample holder.

III.4 Internal photoemission: Schottky barrier height measurements

The internal photoemission technique is an accurate and direct method to determine Schottky barrier heights [Sze 1981] . When a monochromatic beam of light is incident on a metal-semiconductor sample surface, a photocurrent may be generated and measured using a setup as shown in Fig. III.2. In our mesurements, the incident light coming from a tungsten lamp crosses a double-monochromator, is modulated by a chopper and reaches the sample surface. Signal from the sample is measured using a lock-in amplifier. Monochromator and data acquisition are controlled by a dedicated software. All measurements were performed at room temperature.

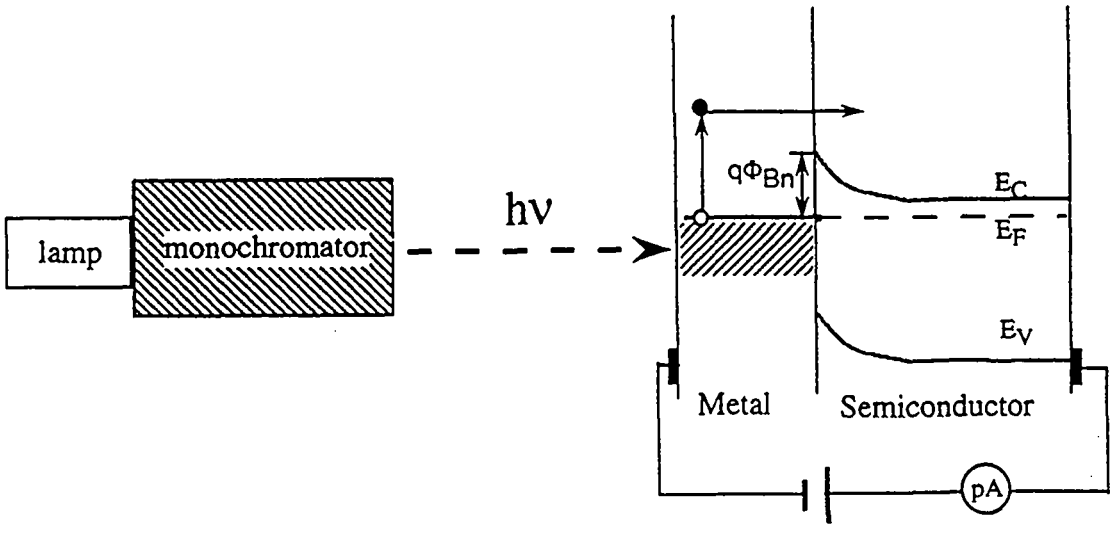


Fig.III.2 - Setup for internal photoemission measurements.

In Fig. III.2 the sample is shown in front illumination configuration. However, for this kind of measurement, another configuration, the back illumination, can be performed.

The front illumination configuration was used for our samples with very thin PtSi layer (3 - 5 nm) and the back illumination for thick silicide samples with interfacial oxide (PtSi thickness ~ 20 nm). The reason lies in the metallic layer (PtSi + residual Pt) morphology: these films show strong texture, with large unreacted Pt islands on the surface. Furthermore, inhomogeneities in thickness change from a sample to an another. The photoresponse, in the front illumination configuration, might be affected by these thickness inhomogeneities. In order to change the signal intensity, a bias of +1V or -1V was applied at the metal surface (in the front illumination configuration) or at the semiconductor surface (in the back illumination configuration).

The photoresponse as a function of the photon energy spectra for all samples show a considerable emission from the tail of the Fermi distribution in the metal. This is correlated to the thickness range (thickness < 30 nm) of the metallic film, as previously reported by Crowell et al. [Crowell 1962]. For this reason data were analyzed using Fowler's model [Fowler 1931]. The photocurrent per absorbed photon R as a function of the photon energy, hν, is given by:

$$R(x) = e^{x} - \frac{e^{2x}}{2^{2}} + \frac{e^{3x}}{3^{2}} - \ldots \qquad \text{for } x < 0$$

$$R(x) = \frac{x^{2}}{2} + \frac{\pi^{2}}{6} - \left(e^{-x} - \frac{e^{-2x}}{2^{2}} + \frac{e^{-3x}}{3^{2}} - \cdots \right) \qquad \text{for } x \geq 0$$

eq.1

where $x \equiv h(\nu - \nu_0)/kT$, hν is the photon energy and $h\nu_0$ is the barrier height ($q\phi_{Bn}$). We fitted the square root of the photoresponse yield (experimental measurements) as a function of hν with $(R(x))^{1/2}$ from eq. 1 to obtain the Schottky barrier height $h\nu_0$. Furthermore, we compare the photoresponse intensity obtained from different samples.

By this way, we have obtained the evolution of the Schottky barrier height and the relative photoresponse intensity as a function of the annealing temperature for 20 nm-thick platinum silicide films with and without interfacial oxide layer as well as for ultrathin films. Results have been correlated to the resistivity values and the morphological and crystallographic evolution of the samples.

III.5 Four-point probe resistivity measurements

The "four point probe" technique is a very convenient tool for resistivity measurement [Smits 1958]. This method, first described by Valdes [Valdes 1954], and generalized by Uhlir [Uhlir 1955], gives the functional relationship between the resistivity, ρ, and the voltage to current ratio (V/I) for various geometries. The conditions are:

a) in-line four-points probe;
b) equal spacing (S) between points;
c) ratio of samples diameter to probe spacing (d/S) >> 1

The sheet resistivity is obtained by [Smith 1958]:

$$\rho_s = (4.5324...)\,\frac{V}{I}$$

where I is the current applied between two outside points, V is the potential difference measured between the two inner points, multiplied by a geometrical factor.

For very small conductive layer thickness ω ($\omega < 300$ μm, in practical terms), as in the case of our samples (where $\omega \leq 20$ nm) the resistivity is given simply by [Wolf 1976]:

$$\rho = (4.5324.\ \omega)\ \frac{V}{I} \qquad [\mu\Omega.cm]$$

The sheet resistance (R_s) is related to the resistivity ρ by:

$$R_s = \rho/\omega \quad [\Omega/\square]$$

The quantity R_s is given in ohms per square ($\Omega/\square$) and is, in fact, the resistance of a square of the film, i.e., the length of the film times the equal width.

The four-point head is a "Alessi Industries" model with distance S between points of ~ 1 mm. The programmable current source was a Keithley-220 model; voltage was measured with a digital multimeter Keithley-195A. Samples were square shaped (d ~ 15 mm and thus, d/S ~ 15 >>1, satisfying the condition (d/S) >> 1).

An additional multimeter connected to the poles of the current source has measured the potential difference V' generated when a current was applied at the sample surface. It gives information about the morphology of the film in the following way: for a metal-like, continuous and conductor film, V and V' are ~ mV or smaller; for partially discontinuous films, (as we will see in Chapter V), measured values for V

and V' increase of a factor 2 or 3 (slight discontinuity) up to 10 - 12, as in the case of micelle-like films (see Chapter V). When the silicide film becomes discontinuous, V suddenly decreases but V' increases even more, indicating that the current no longer passes through a conductor film, but through a n-type semiconductor medium, the Si substrate. V decreases because the layer thickness is no longer a few nanometers-thick, as in silicide films, but the whole thickness of the Si substrate, i.e., 590 μm. In fact, using the measured V and ω = 590 μm for ρ calculations, we obtain the Si substrate resistivity. Thus, measuring V' is fundamental to interpret our resistivity results as a function of the annealing temperature and to detect the temperature in which the film becomes discontinuous.

REFERENCES

[Crowell 1962] C.R. Crowell, W.G. Spitzer, L.E. Howarth and E.E. LaBate, Phys. Rev. **127**(6), 2006 (1962).

[Edington 1975] J.W. Edington, "Electron Diffraction in the Electron Microscope", Philips Technical Library (1975).

[Fowler 1931] R.H. Fowler, Phys. Rev. **38**, 45 (1931).

[Heimendahl 1980] M. von Heimendahl, "Electron Microrscopy of Materials", Academic Press, New York (1980).

[Hirsch 1967] P. Hirsch in "Electron Microscopy of Thin Crystals", Florida (1967).

[Ishizuka 1980] K. Ishizuka, Ultramicroscopy **5**, 55 (1980).

[Mollendstedt 1987] G. Mollendstedt and F. Lenz, Adv. Electron. Phys. **18**, 251 (1963)

[Reimer 1984] L. Reimer, "Transmission Electron Microscopy", Springer-Verlag, Berlin (1984).

[Smits 1958] F.M. Smits, The Bell System Technical Journal **XXXVII**(3), 711 (1958).

[Spence 1981] J.C.H. Spence, "Experimental High-Resolution Electron Microscopy", Oxford University Press, Oxford (1981).

[Stadelmann 1987] P.A. Stadelmann, Ultramicroscopy **21**, 131 (1987).

[Sze 1981] S.M. Sze, "Physics of Semiconductors", 2nd edition, J. Wiley & Sons (1981).

[Tonner 1988] B.P. Tonner and G.R. Harp, Rev. Sci. Instrum. **59**(6), 853 (1988).

[Tonner 1989] B.P. Tonner and G.R. Harp, J. Vac. Sci. Technol. **A7**(1), 1, (1989).

[Tonner 1990] B.P. Tonner, Nucl. Instr. and Meth. **A291**, 60 (1990).

[Uhlir 1955] A. Uhlir Jr., Bell Syst. Tech. J. **34**, 105 (1955).

[Vainshtein 1964] B.K. Vainshtein, "Structure Analysis by Electron Diffraction", Pergamon Press (1964).

[Valdes 1954] L. Valdes, Proc. IRE. **42**, 420, (1954).

[Wolf 1976] H.F. Wolf, "Silicon Semiconductor Data", 2nd edition, Pergamon Press, Oxford (1976).

Chapter IV

Pt - Si Reaction with Interfacial Native Silicon Oxide Layers

In this Chapter we investigate the formation of platinum silicide films in the presence of interfacial native oxide films as well as on oxide-free silicon wafers. The influence of the interfacial oxide layer on the Pt - Si reaction was examined as a function of the annealing temperature, from the early stages (at low temperatures) up to the complete degradation of the films (at high temperatures). We compare the evolution of the silicide films with interfacial oxide layer to that of an oxide-free sample, prepared at the same annealing conditions to establish the role of the native oxide layer in the Pt - Si reaction.

Characterizing these films in detail is delicate: a sub-nanometric resolution in the measurements is necessary. HRTEM is a technique able to give us simultaneously morphological, structural and crystallographic information with atomic resolution. These capabilities enabled us to describe the evolution of silicide films with annealing temperature and, in particular, how morphological and crystallographic transformations occur. The Pt-Si phases present in the silicide layer and their spatial distributions are described for each annealing temperature. The degree of continuity and homogeneity is evaluated in each case. Transformations of the residual non-reacted Pt layer and of the interfacial native oxide were also studied.

On the other hand, the Photoelectron Microscopy (PEM) is able to give chemical information about the samples. It confirms the phase description obtained by electron diffraction and HRTEM, in analyses taken over a large area of the samples (several tenths of μm). This is an important feature that shows the extent of the homogeneity of our samples and the validity of the results.

IV.1 Experimental procedure

20 nm-thick platinum silicide films with and without interfacial native silicon oxide layer were obtained by sputtering deposition and thermal annealing at various temperatures as described in Chapter II. For TEM imaging, planar-view and cross sectional samples were prepared by standard microscopy preparation techniques: manual mechanical polishing followed by ion milling. The microscope was a Philips EM 430 ST instrument, with a resolution better than 0.20 nm, as mentioned in Chapter III. The data analysis was based on the software developed by P. Stadelmann [Stadelmann 1987] .

For PEM analyses, samples were cleaved to the appropriate dimensions to be put in the sample holder. The photoelectron microscope used in this work was developed by Tonner and co-workers ([Tonner 1988]; [Tonner 1989]; [Tonner 1990]) as described in Chapter III.

IV.2 Platinum silicide formation and evolution as a function of the annealing temperature investigated by HRTEM

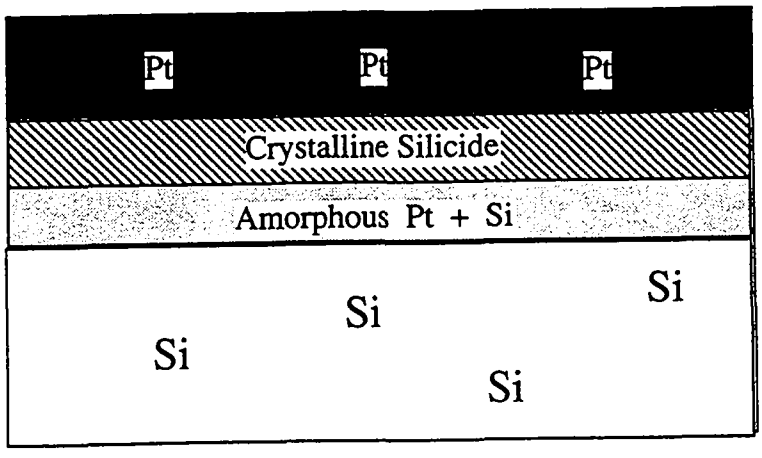
In this section we describe how RF-sputtered platinum films, prepared as described in Chapter II, react with silicon atoms from the substrate, in oxide-free substrates and in samples with the interfacial native silicon oxide layer (1.3 ± 0.2 and 2.2 ± 0.3 nm-thick). The steps of the Pt - Si reaction were analyzed by electron microscopy techniques. The morphology evolution is described by a sequence of planar-view low-magnification micrographs: grain formation and size changes as well as film continuity are observed in this kind of sample imaging. The electron diffraction (ED)

patterns were obtained from the same area, giving the crystallographic phases present at each annealing temperature. The phase distribution in the volume of the silicide film was identified in HRTEM cross-sectional images that also give details of the Pt-Si reaction and the evolution of silicide/silicon interface. Tables with a complete description of all identified phases including their crystallographic orientation at each annealing temperature can be found in Appendix 1.

IV.2.1 Early stages of the Pt-Si reaction

Si substrates were heated at 165 °C and kept at this temperature for 30 minutes before and during deposition. This treatment initiate the Pt-Si reaction, forming metal-rich silicide phases on oxide-free and 1.3 nm-thick oxide samples; 2.2 nm-thick interfacial oxide provides very low Pt supply and the Pt-Si reaction was seen at its first step, i.e., as a sub-nanometric Pt + Si amorphous layer at the substrate surface, below the oxide. It is clearly observed that, from the first steps, the reactant diffusion proceeds through the oxide pinholes. The Pt-Si reaction mechanism and phase formation as well as island formation mostly depend on the flow rate of reactants and, consequently, on the pinhole density.

In Fig. IV.1.a we can see the as-deposited Pt film on an oxide-free substrate (sample X). At the top, the unreacted Pt film covers the silicide layer. The unreacted Pt layer is 6.0 nm-thick while 9.0 nm of platinum silicide have already formed. The silicide layer contains, in fact, two sub-layers: a partially crystallized sub-layer, in the vicinity of the Pt interface, and an amorphous layer at the silicide/Si interface, previously seen by Abelson et al. [Abelson 1988]. The phase distribution is schematically represented below:

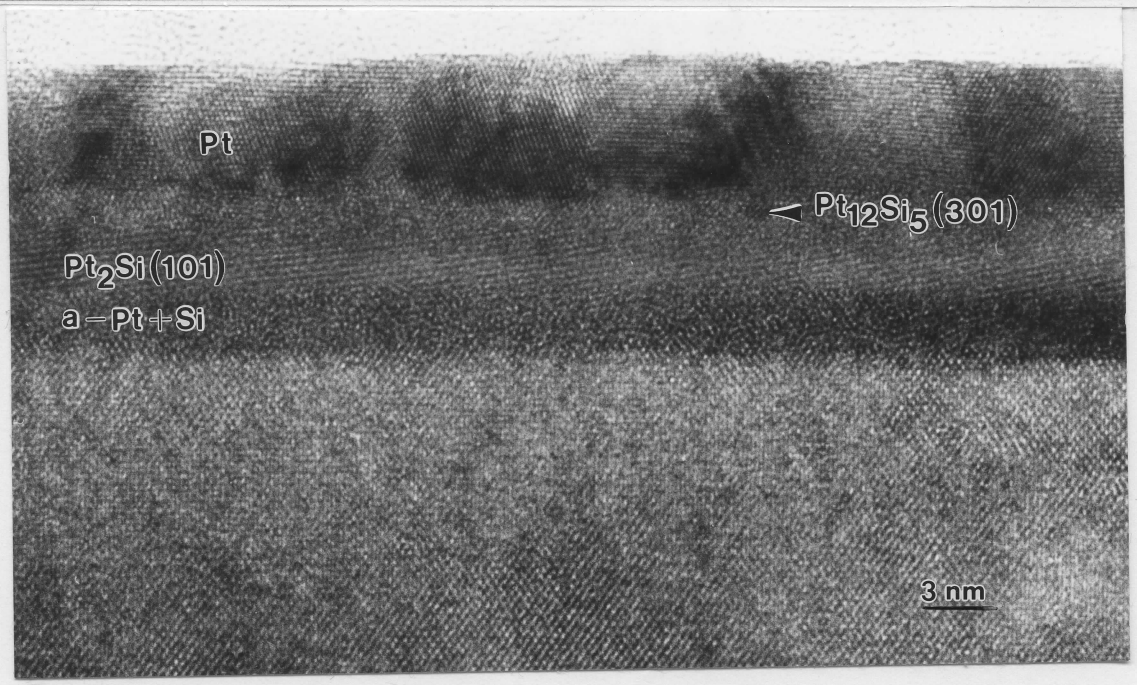


Schematic representation of Fig. IV.1a

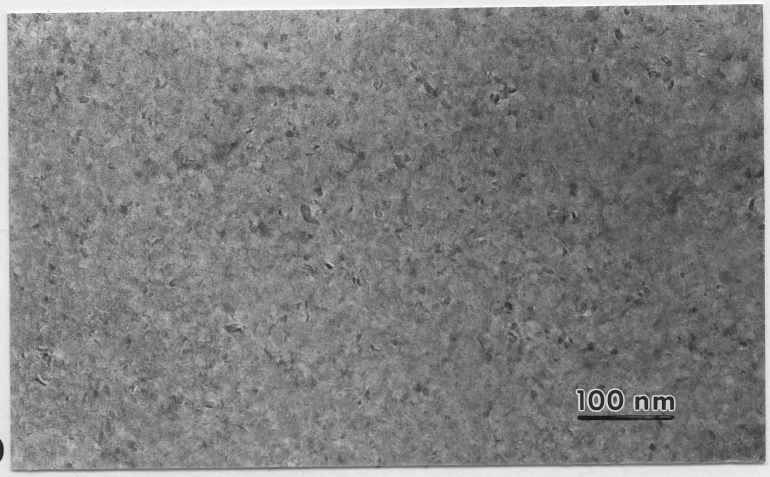
The silicide/silicon interface is flat. In the partially crystallized sub-layer we can identify two metal-rich silicide phases: $Pt_2Si(101)$ planes and $Pt_{12}Si_5(301)$ planes. The two silicide phases, first identified by electron diffraction, are confirmed by HRTEM, by measuring the distance between atomic planes. The ED pattern (Fig. IV.1.c), shows that this layer, as well as the unreacted Pt layer, are polycrystalline, as indicated by the rings. Planar-view observations (Fig. IV.1.b) show a continuous film formed by small grains with a grain size of ~ 10 nm, that is very similar to the as-deposited **Y** (with 1.3 nm-thick interfacial oxide layer) and **Z** (with 2.2 nm-thick interfacial oxide layer) samples (figs. IV.2 and IV.3, respectively).

It is important to clarify that the *Pt_2Si* phase we are talking about is, actually, *α-Pt_2Si*, the tetragonal phase with a = b = 0.393 nm and c = 0.591 nm. A β-Pt_2Si is predicted by the phase diagram, but it was not observed in this work; thus, for simplicity, we will use "Pt_2Si" instead of "α-Pt_2Si" unless we refer explicitly to the "β" phase.

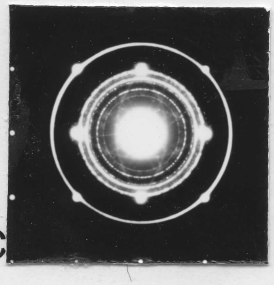
The Pt-Si reaction is also observed in the sample Y, with 1.3 nm-thick interfacial oxide layer (Fig. IV.2.a). In this case, the atomic migration to produce



a



b



c

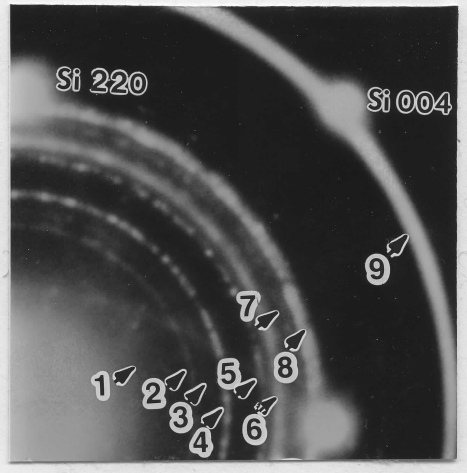
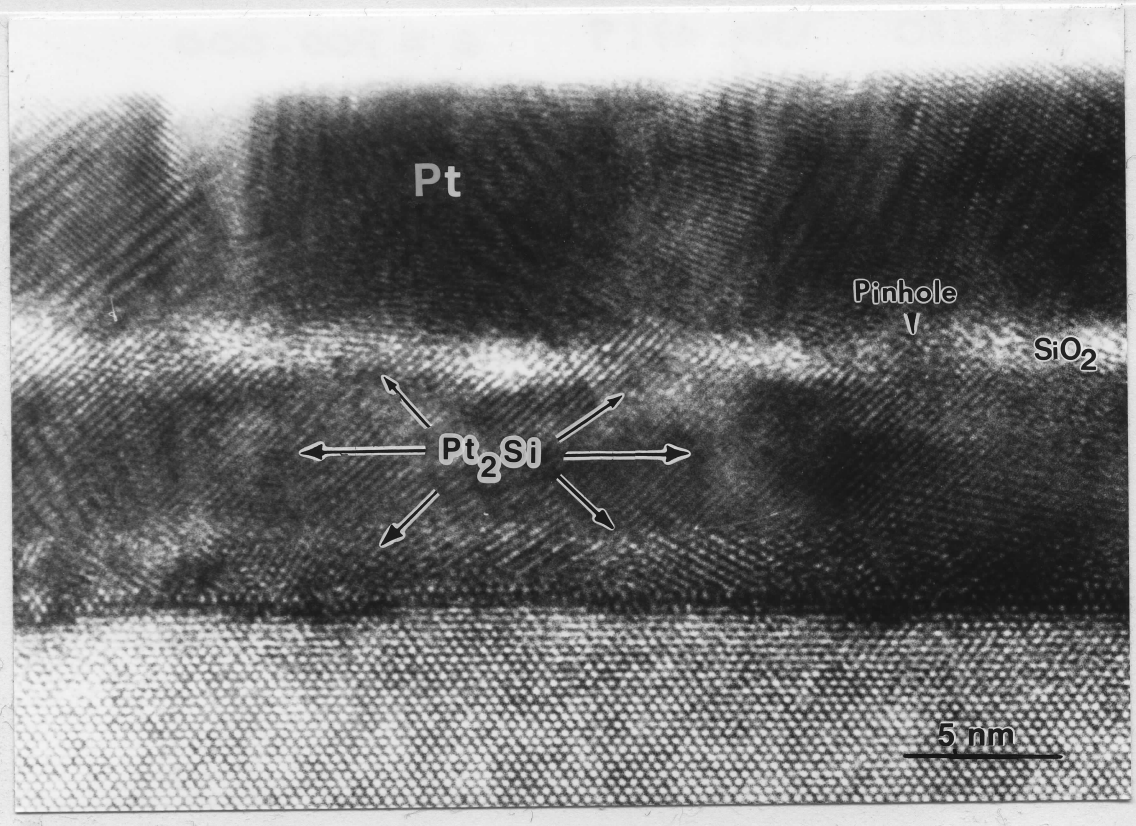
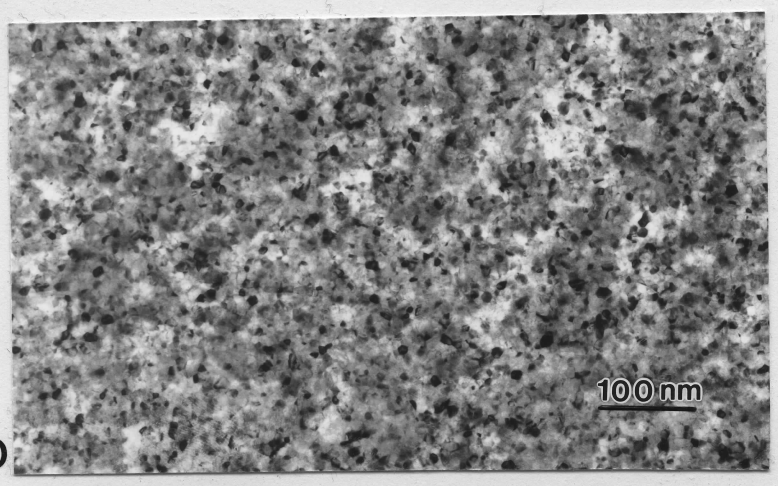


Fig. IV.1 - TEM images of sample X, as-deposited. a) HRTEM cross-sectional image showing the unreacted Pt and the silicide (crystallized and amorphous) layers and the Si substrate; b) Planar-view image; c) ED pattern: general view at left and a detail at right. Numbered arrows point to rings indicating: 1-3-5: $Pt_{12}Si_5$ phase; 2-4-7: Pt_2Si phase; 6-8-9: unreacted Pt.



a



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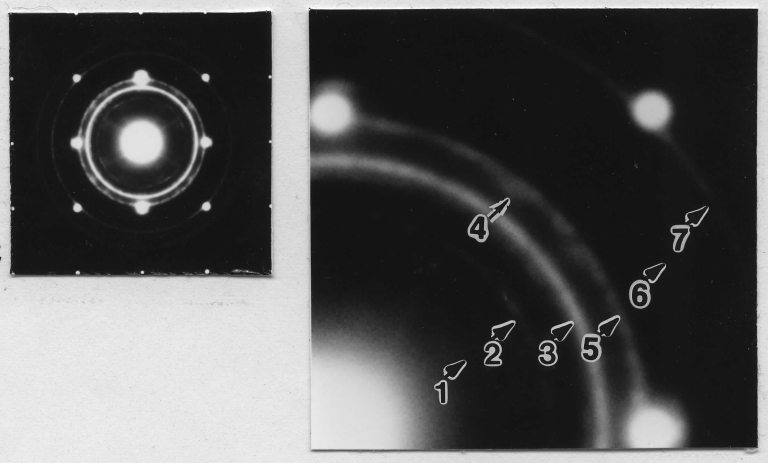


c

Fig. IV.2 - TEM images of sample Y (with 1.3 nm-thick interfacial oxide), as-deposited. a) HRTEM cross-sectional image; b) Planar view image; c) ED pattern, a general view at left and a detail at right. Arrows indicate: 1-2-4-6: Pt_2Si phase; and 3-5-7: unreacted Pt.

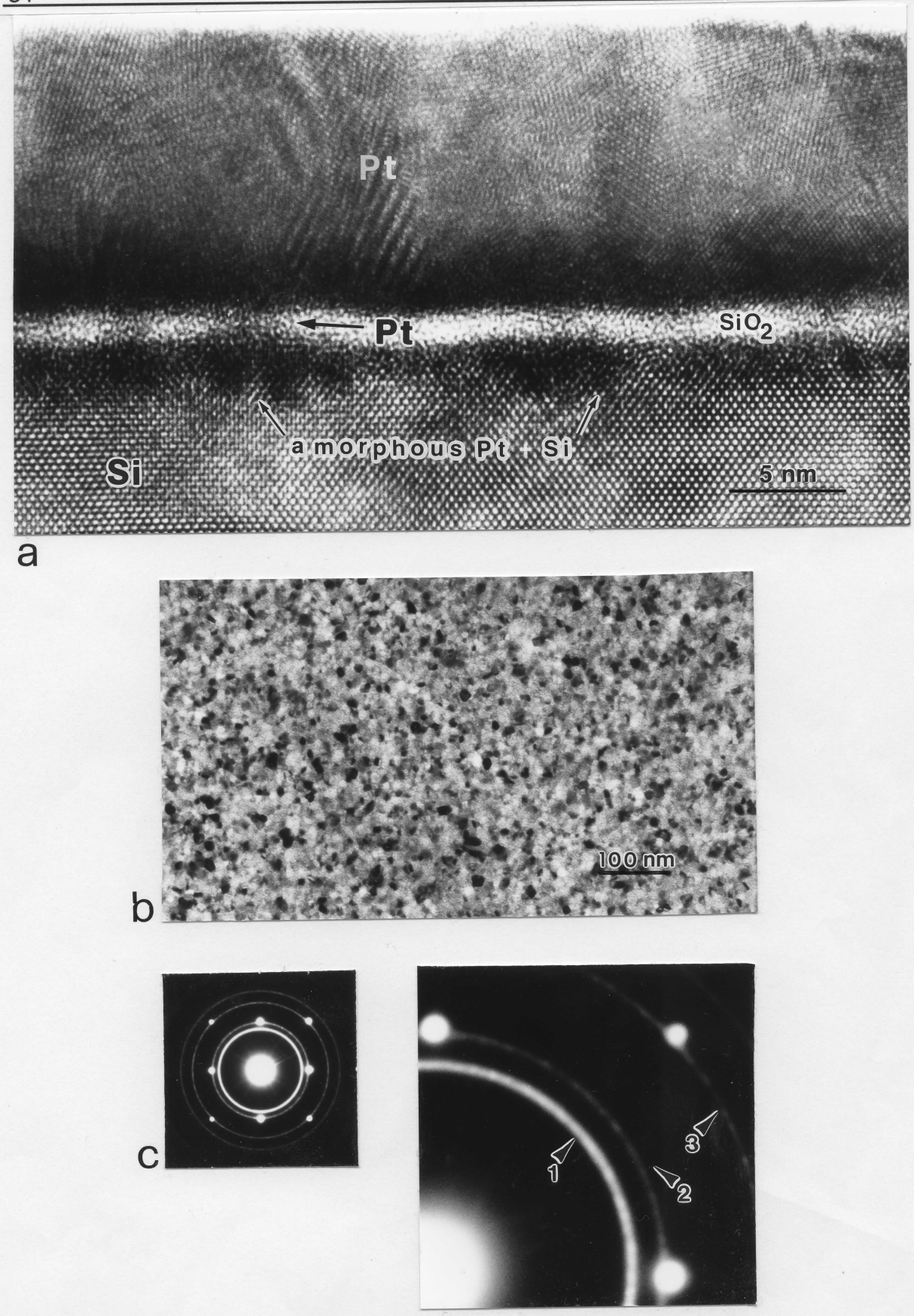
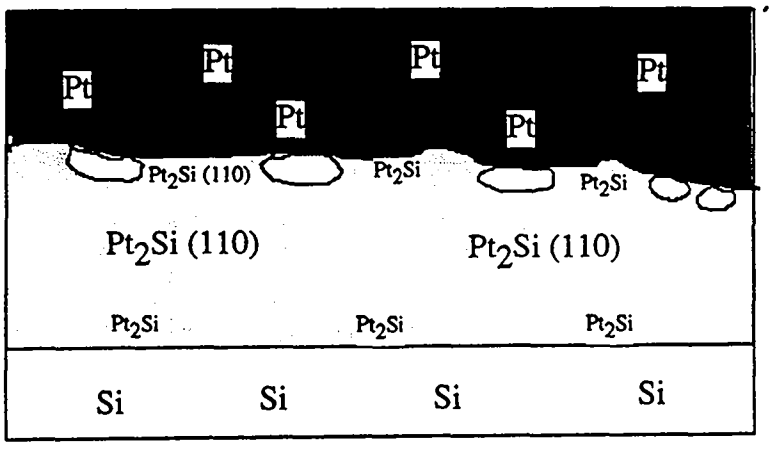


Fig. IV.3 - TEM images of sample Z (with 2.2 nm-thick interfacial oxide), as-deposited. a) HRTEM cross-sectional image; b) Planar-view image; c) ED pattern, general view at left and a detail at right. Arrows indicate: 1-2-3: unreacted Pt.

the Pt-Si reaction occurs through the pinholes present in the oxide layer. In the 1.3 nm-thick oxide layer, the large number of pinholes present allows the atoms to migrate easily and many nucleation centers contribute to the silicide formation. The mean pinhole separation is 2.0 nm. Thus, the high oxide pinhole density can guarantee a moderate Pt supply. The silicide layer formed is quite similar to that obtained in the oxide-free case. The only difference is the absence of the amorphous silicide sub-layer. This is explained by the reaction speed, that is decreased by the oxide layer, and allows the atoms to take place. We identified a Pt_2Si silicide phase present in the interior of the pinholes, showing atomic planes in the [110] direction, which are connected to sub-grains in the silicide film below the oxide layer. These sub-grains are also formed by Pt_2Si with atomic planes in the [110] direction, randomly oriented with respect to the substrate. We show, below, a schematic representation of the silicide phase distribution in the film, as well as the silicide/Si interface obtained:

The silicide layer formed in as-deposited conditions already reach more than a half of its final thickness. The interface with silicon is smooth with steps. In fact, even a 165 °C annealing appears sufficient to produce a continuous silicide film with a flat diffusion front. As we will see, this is not possible for larger oxide thicknesses. In the ED pattern (Fig. IV.2.c), we can identify two metal-rich silicide phases, Pt_2Si and



Schematic representation of Fig. IV.2a

$Pt_{12}Si_5$. The other rings belong to unreacted Pt. Morphologically, this film is similar to sample X, with grains of 10 nm in size (planar-view image, Fig. IV.2.b).

Figure IV.3.a shows a metallic Pt layer over a homogeneous (2.2 ± 0.3 nm-thick) amorphous native oxide film. This layer completely covers the substrate surface and no regions of direct contact between Pt and Si are found. We can see the diffusion through the pinholes of the oxide, as a consequence of Pt migration into Si. The average pinhole distance is 8.0 nm, four times larger than in the 1.3 nm-thick oxide case. Small quantities of amorphous platinum silicide form at the substrate surface. No evidence of crystalline platinum silicide was found. The silicide layer is not continuous yet, but formed by Pt + Si agglomerates correlated to oxide pinholes as a consequence of the reduced number of nucleation centers and slow Pt supply. This is clearly the *first step* of the Pt - Si reaction. Note that the formation of this amorphous layer occurs *below* the native oxide film. This result confirms that platinum does migrate faster than Si in agreement with several authors ([Tu and Mayer 1978]; [Ottaviani 1979]; [Ottaviani 1986]; [Tsui 1990]). Furthermore, the migration does occur through pinholes in the oxide, which are present even for a 2.2 nm-thick oxide layer. The ED pattern (Fig. IV.3.c) does not show any crystalline silicide phase. Only rings belonging to polycrystalline, unreacted, Pt are seen.

Thus, in this early stage of Pt - Si reaction, we observe the importance of the contact area between the reactants in defining the degree of development that the reaction can reach. For the same deposition temperature and heating time, we observed large differences between samples with and without oxide barrier: we can see the Pt-Si reaction at its first step, i.e., isolated nucleation regions of amorphous Pt + Si under 8 nm-far pinholes, until a half-reacted Pt layer forming an amorphous + double phase polycrystalline film if reactants are in full contact. As we will see in the next paragraph, pinholes play an important role over the whole range of low-temperature annealing (up to 250 °C).

The evolution between as-deposited and 250 °C-annealed samples can be observed by comparing Fig. IV.1,2,3 and Fig. IV.4,5,6. Morphologically, the three samples are quite similar at 250 °C, formed by grains shaped like polyhedrons with grain size between 10 - 20 nm (planar-view images, Fig. IV.4b, 5b and 6d).

The ED pattern obtained from the same areas for the three samples show, however, different set of silicide phases forming each silicide film:

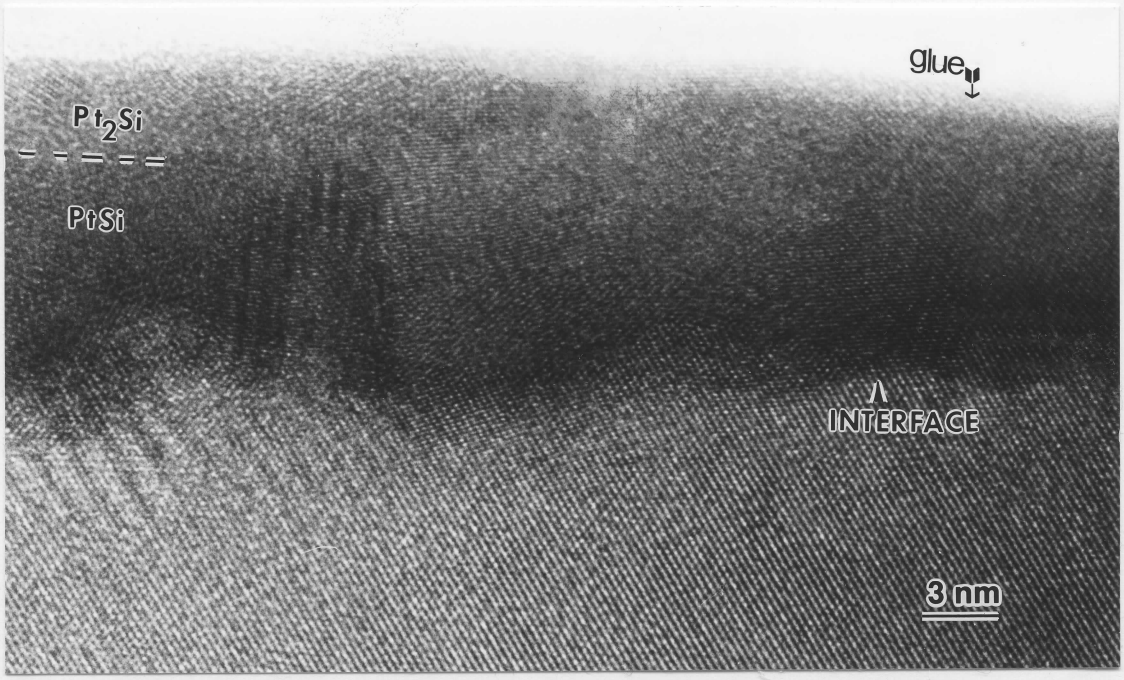
- sample X (without oxide): Pt_2Si and PtSi phases (Fig. IV.4.c);

- sample Y (1.3 nm-thick interfacial oxide): $Pt_{12}Si_5$ (very few), Pt_2Si (large quantity) and unreacted Pt (Fig. IV.5.c);

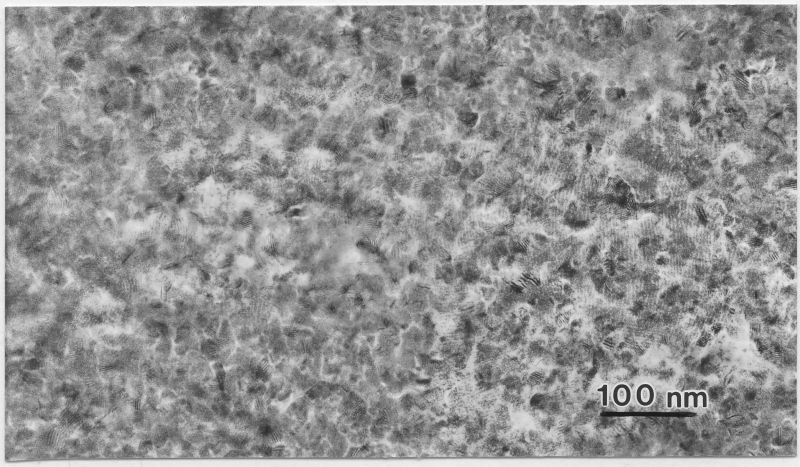
- sample Z (2.2 nm-thick interfacial oxide): $Pt_{12}Si_5$, Pt_2Si, PtSi and unreacted Pt (Fig. IV.6.e).

For samples X and Y we identify only rings, indicating that the phases present in these samples are polycrystalline. For sample Z, however, only $Pt_{12}Si_5$ phase is polycrystalline (identified by some rings in the ED); Pt_2Si and PtSi show some epitaxial order (ED pattern constituted by rings and spots). Sample X is constituted by metal-rich and stable silicide phases; sample Y, only by metal-rich silicide and unreacted Pt; and finally, sample Z, by all silicide phases (and unreacted Pt) showed by the other two. To understand the mechanism that leads to the formation of such phase sequences, let us examine their spatial distribution in the cross-sectional images.

The cross-sectional image of sample X annealed at 250 °C is shown in Fig. IV.4.a. The original Pt layer has fully reacted and only the silicide layer is found. Its thickness is already the definitive at 250 °C, i.e., 22 nm. The silicide layer is well-crystallized and formed by two sub-layers, Pt_2Si (at the top) and PtSi (between the Pt_2Si sub-layer and the Si substrate), forming a rough interface with the Si substrate.



a



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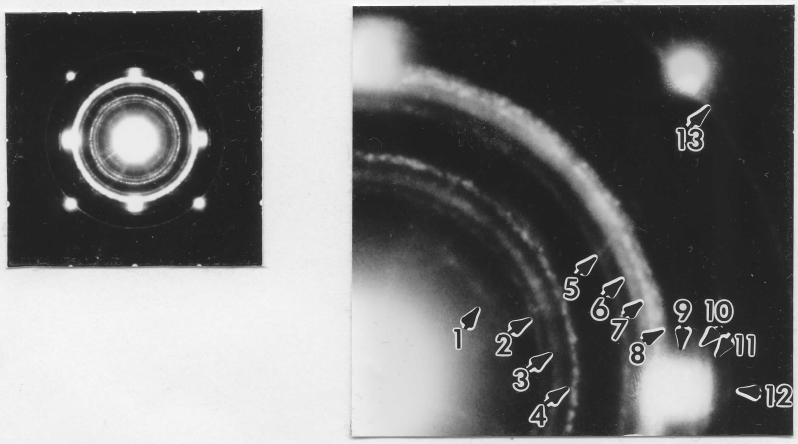


c

Fig. IV.4: TEM images of sample X annealed at 250 °C. a) HRTEM cross-sectional image. b) Planar-view image. c) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-3-5-6-7-8-10-11: PtSi phase; 2-4-9-12: Pt_2Si phase.

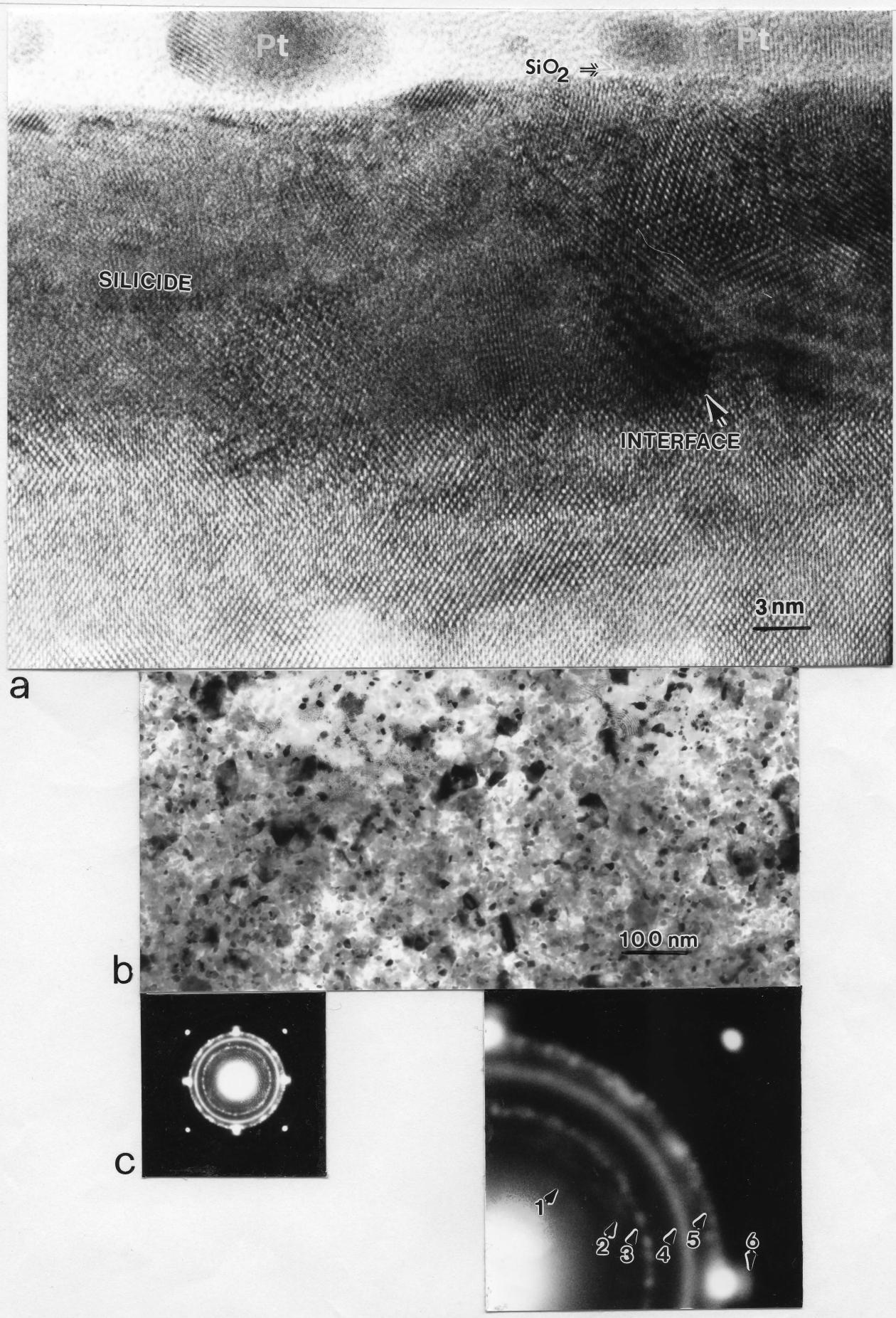


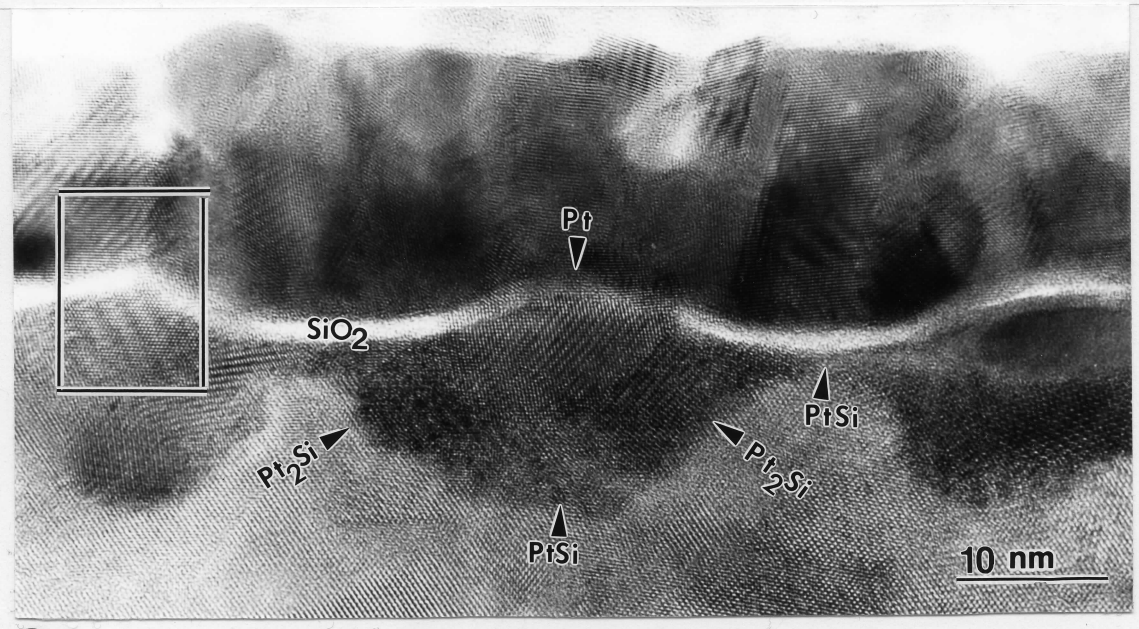
Fig. IV.5: TEM images of sample Y annealed at 250 °C. a) HRTEM cross-sectional image. b) Planar-view image. c) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-2-3-6: Pt_2Si phase; 4-5: unreacted Pt.

We can even detect short range ordered PtSi. These results show that the reaction: $Pt_2Si + Si \rightarrow 2PtSi$ is in progress and even in an advanced state in this sample annealed at 250 °C.

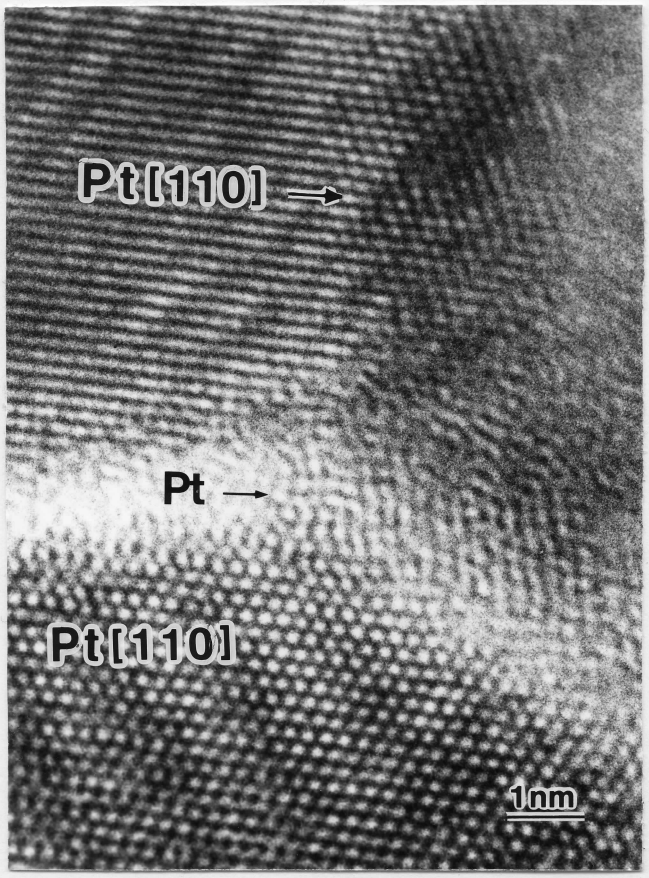
The presence of these two phases, and only these two, is confirmed by the ED pattern (Fig. IV.4.c). Both phases show rings only, indicating that they are polycrystalline.

Examining the cross-sectional image of sample Y annealed at 250 °C, we observe that the larger part of the original metallic Pt film has diffused through the pinholes of the 1.3 nm-thick interfacial oxide and has reacted (Fig. IV.5.a). The silicide phases formed are metal-rich, i.e., $Pt_{12}Si_5$ and Pt_2Si. We observe that the silicide/Si interface and the substrate surface are quite smooth and flat and no volume increase at the silicide/SiO_2 interface is found. We found only $Pt_2Si(101)$ grains in the silicide film at the silicide/Si interface. On the other hand, the few $Pt_{12}Si_5$ grains found are localized at the Pt_2Si/Pt interface. The grain boundaries, however, are not well defined even at 250 °C; amorphous platinum silicide is visible among well crystallized Pt_2Si and $Pt_{12}Si_5$ regions.

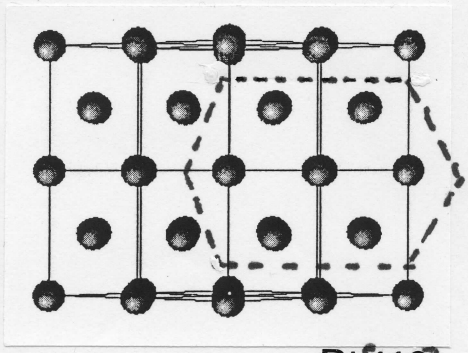
The cross-sectional image in Fig.IV.6.a (2.2 nm-thick interfacial oxide layer) clearly shows (111) atomic planes belonging to the crystallized unreacted Pt *inside* the oxide pinholes (e.g., in the central pinhole in the Fig. IV.6.a). We also found sub-grains formed by unreacted Pt in [110] zone axis just *below* the oxide layer, close to the pinholes. A detail of the cross-sectional image (Fig. IV.6b) shows, in high magnification, sub-grains formed by unreacted Pt in [110] zone axis *in* the *unreacted Pt layer* and *in* the *silicide agglomerate.* We can compare this image with the projected image of the Pt structure in the [110] zone axis (Fig. IV.6c). The schematic representation of the silicide phase and unreacted Pt distribution in the silicide agglomerates, oxide pinholes and in the 'horizontal bridges' connecting the agglomerates are shown below:



a

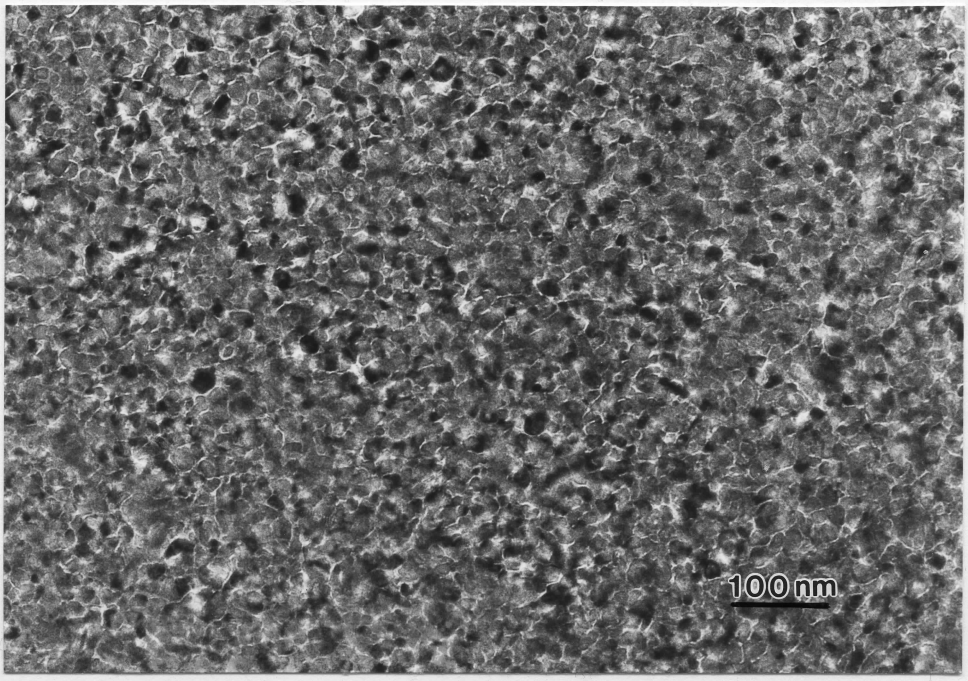


b

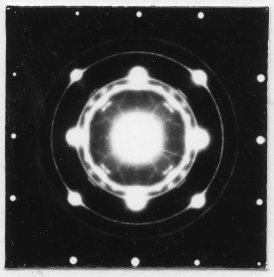


c Pt[110]

Fig. IV.6: TEM images of sample Z annealed at 250 °C. a) HRTEM cross-sectional image, general view. At the center, we can see a pinhole crossed by atomic planes (Pt(111)). b) Detail of the image in a), showing the unreacted Pt above and below the oxide layer crossing an oxide pinhole. In particular, Pt grains can be found above and below the pinhole in the same orientation, Pt[110]. c) Projection of the Pt structure in the [110] zone axis.



d



e

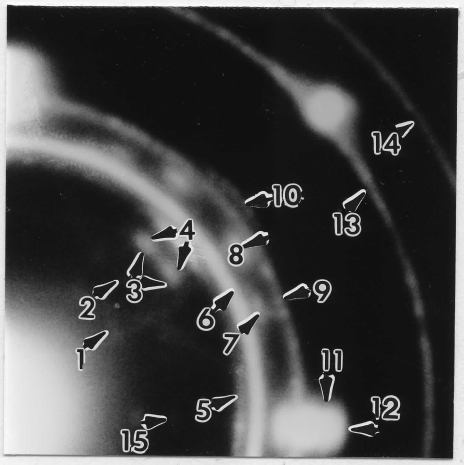
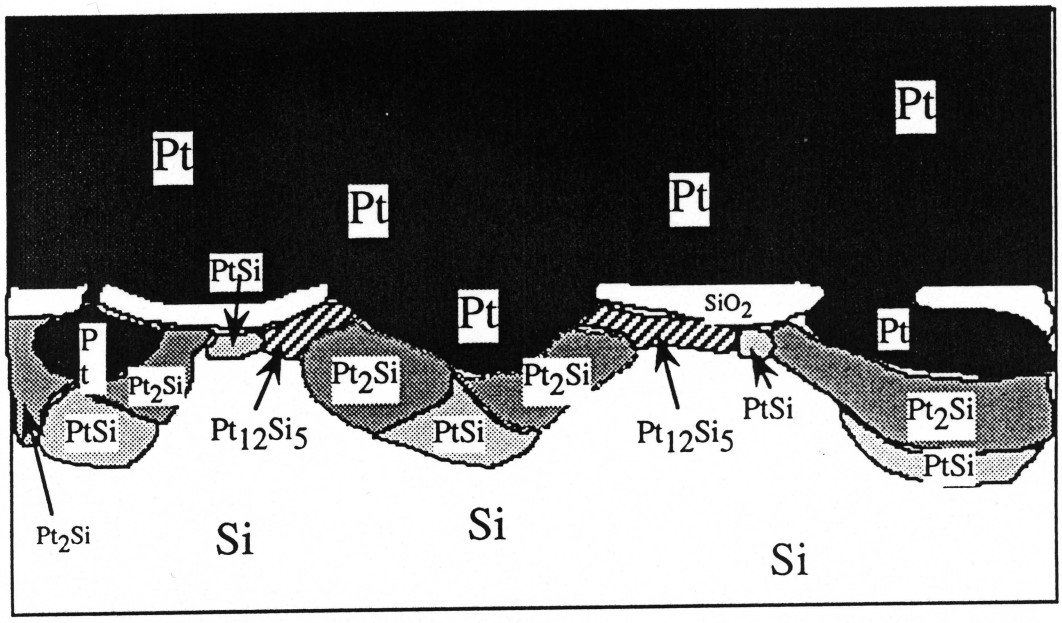


Fig. IV.6 (cont.): d) Planar-view image of sample Z annealed at 250 °C. White lines between grains indicate the amorphization of the grain boundaries. e) Corresponding ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-3-4-7-8-9-11-12: PtSi phase; 2-15: Pt_2Si phase; 5-10: $Pt_{12}Si_5$ phase; and 6-13-14: unreacted Pt.



Schematic representation of Fig. IV.6a

Beyond the unreacted Pt sub-grains, the agglomerates below each pinhole are constituted mainly by two silicide phases: Pt_2Si and PtSi. The Pt_2Si phase, represented by sub-grains in [0,-1,0] or [-1,-1,0] zone axis, is found inside the round agglomerates laterally with respect to PtSi sub-grains and between PtSi (at the interface with silicon) and Pt (just below the pinholes), vertically. On the other hand, PtSi, that can be found in [0,0,-1] or [1,1,0] zone axis at the silicide/silicon interface, progressing towards the Si surface through the center of the agglomerate. It is also found in the center of the horizontal bridges connecting two silicide agglomerates, which form below the oxide pinholes. In the last case, PtSi is formed due to Pt lateral diffusion.

The silicide phases present in the bridges are: metal-rich ($Pt_{12}Si_5$ or Pt_2Si) near the bottom of the two pinholes connected by the bridge, and the stable PtSi at the center. Some $Pt_{12}Si_5$ sub-grains can be found between PtSi and Pt grains or even between Pt_2Si and Pt grains. A small quantity of amorphous silicide platinum is still present. Due to the localized silicide agglomerate formation, the substrate surface is

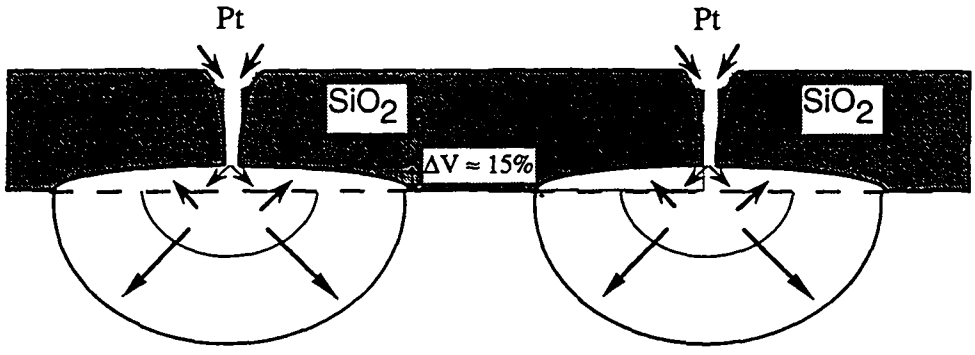
no longer flat. The deformation at the Si/SiO_2 interface over a silicide agglomerate is approximately 10 - 15%.

We discussed the role played by the density of the oxide pinholes in the Pt - Si reaction. The density of oxide pinholes has also an influence on the flatness of the silicide/Si interface. We discuss this point below:

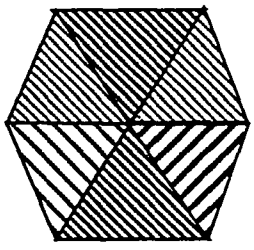
In the oxide-free case (sample X), the continuity of the developing silicide film and the silicide/Si interface flatness are easy to understand: Pt and Si are in full contact, and the diffusion (and reaction front) progress at the same speed over all the sample.

For samples with an interfacial oxide which acts as a barrier to the reactant diffusion, the silicide/Si interface flatness depends mainly on the distance between the pinholes in the oxide layer. Just below each pinhole of the oxide layer we find, in the substrate, a rounded interdiffusion (and reaction) region. If the pinholes are far enough from each other (8.0 nm, for instance), these rounded regions (or agglomerates) do not overlap and they can be seen isolated. They are connected only by a very narrow silicide layer, formed by lateral Pt diffusion. A top view of these regions shows agglomerates as polyhedrons; a cross sectional view allows us to realize that the observed polyhedrons are, in fact, just the upper part of the — very roughly speaking — drop-like reaction agglomerate. The polyhedrons have the form of a hexagonal pyramid; their basis lies in the plane of the metal/SiO_2 interface. The growth of a pyramidal region corresponds to the volume increase mentioned (10 - 15%). The rounded region, below the pyramid, is roughly a half-sphere.

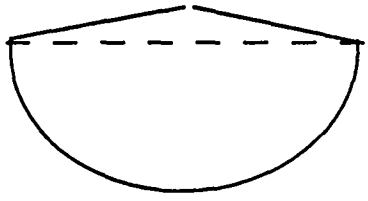
If pinholes are close to each other (2.0 nm, for instance), the distance between pinholes being equal or smaller than the diffusion depth, the rounded regions overlap. The result is a flat diffusion front and homogeneously distributed reactant interdiffusion, and consequently, a flat silicide/Si as well as silicide/SiO_2 interfaces. A schematic illustration of these mechanisms is shown in Fig. IV.7.



Pt-Si reaction region

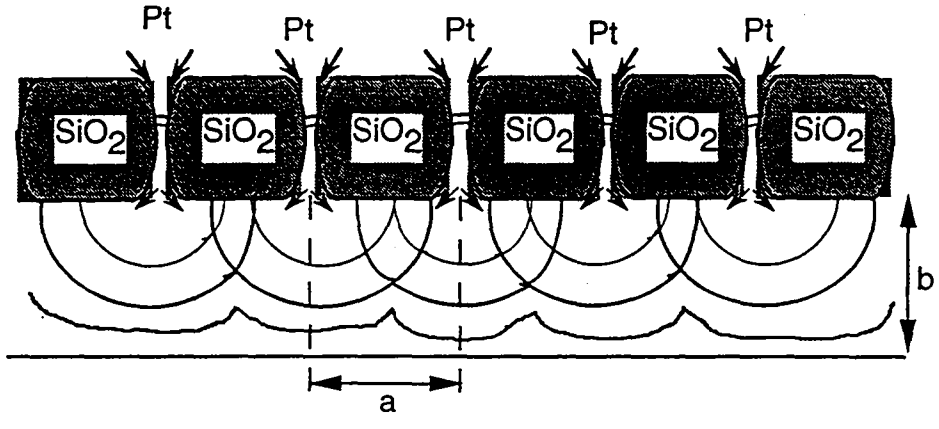


Top-view of the grain



Lateral view of the grain

a)



b) To obtain a flat reaction front: b > a

Fig. IV.7: Schematic representation of the Pt - Si reaction and the resulting reaction front in the samples: a) Z; b) Y.

By comparing our observations with the Pt - Si reaction mechanisms proposed in the literature, one can say that oxide-free samples seems to follow the mechanism proposed by Majni et al. [Majni 1985] (see Chapter II) in the case where the available quantity of Pt atoms is much smaller than that of Si atoms. In this case, the speed of the Pt-Si reaction is limited by that of the $2Pt + Si \rightarrow Pt_2Si$ reaction. Majni et al. (1985), and even former models ([e.g. Tsaur 1981], see Chapter II), predict the following phase distribution: Si / Pt_2Si / Pt (or Si / Pt_2Si, with the consumption of all Pt) up to 250 °C. Furthermore, it is well accepted that the PtSi phase starts to grow at the Pt_2Si/Si interface by the reaction: $Pt_2Si + Si \rightarrow 2PtSi$ only when all platinum is consumed. PtSi formation is observed experimentally at temperatures higher than 250 °C (according Majni et al. [Majni 1985]) or higher than 300 °C (according Tu and Mayer [Tu and Mayer 1978]) due to its activation energy.

In oxide-free samples we first observed the distribution (165 °C): Si / Pt_2Si / Pt and, at 250 °C: Si / PtSi / Pt_2Si (all Pt was consumed). This suggests that Majni's mechanism has been followed, but in the case of our samples the PtSi formation starts at lower temperatures (< 250 °C) than in the case of Majni's samples (> 250 °C).

This discrepancy can be explained by the thickness of the deposited Pt film: Majni used 60 nm-thick Pt films, while ours are 20 nm-thick. We observed that, for thinner Pt films, the available Pt reacts faster with Si than for thicker Pt films (see Chapter V). Furthermore, as we will see in the next section, the transformation of metal-rich phases into PtSi is complete at 350 °C for 20 nm-thick films on oxide-free substrates. This suggests an activation energy for PtSi phase formation lower than that found in the literature (1.6 eV, according [Tu and Mayer 1978]). Unfortunately, we do not have enough data (only values at three temperatures) to obtain a precise value for Pt_2Si and PtSi activation energies and to clarify this point.

The silicide formation is different when a diffusion barrier is present. Due to the reduced Pt supply, the $2Pt + Si \rightarrow Pt_2Si$ reaction progresses more slowly than in oxide-free samples. With a 1.3 nm-thick oxide layer is, the moderate Pt supply

allows the formation of a substantial part of the definitive layer at 250 °C, showing only metal-rich phases. However, some unreacted Pt remains, which will not be completely consumed before 550 - 600 °C, as we will see in the following paragraphs. Furthermore, at the expected temperature (≥ 250 °C) metal-rich phases start to transform to PtSi, *even in the presence of unreacted Pt,* and this last fact is in disagreement with Majni's model.

In the presence of a 2.2 nm-thick interfacial oxide layer, differences in the reaction kinectics are even more remarkable. The reduced reaction speed allowed us to observe small, amorphous, Pt + Si agglomerates (not a layer yet) at 165 °C, as previously reported by Abelson et al. [Abelson 1988] for the Pt-Si reaction, but at lower temperatures. The silicide thickness, in the case of 2.2 nm-thick interfacial oxide, increases more slowly, as a function of the annealing temperature, than in the oxide-free case, in the 1.3 nm-thick oxide case. This means that the silicide film thickness is not only proportional to the square root of the time, as in interdiffusion-controlled formation processes, but also depends on the pinhole density and diameter.

Concerning the phase distribution in the agglomerates, we observe: Si / PtSi / Pt_2Si / Pt (unreacted Pt *below* the oxide layer) or, in some cases, Si / PtSi / Pt_2Si / $Pt_{12}Si_5$ / Pt, that are not predicted by any known silicide formation mechanism. Thus, these agglomerates are formed by an heterogeneous phase distribution across the silicide thickness, from metal-rich phases at the top (in contact with the unreacted Pt layer), and PtSi phase (Si-rich) at the bottom (far from the Pt layer). Consequently the Pt-Si reaction is not homogeneous across the agglomerate, but depends on the local concentration of Pt atoms, which depends, once more, on oxide pinholes density and diameter.

This set of results can also explain certain discrepancies in the values of the preexponential factor D_0 from the Arrhenius plot for the Pt - Si reaction in the literature (see Chapter II). Authors who observed the growth of a single phase at a time (e.g., Wittmer [Wittmer 1983]), found higher values for D_0 than those found by,

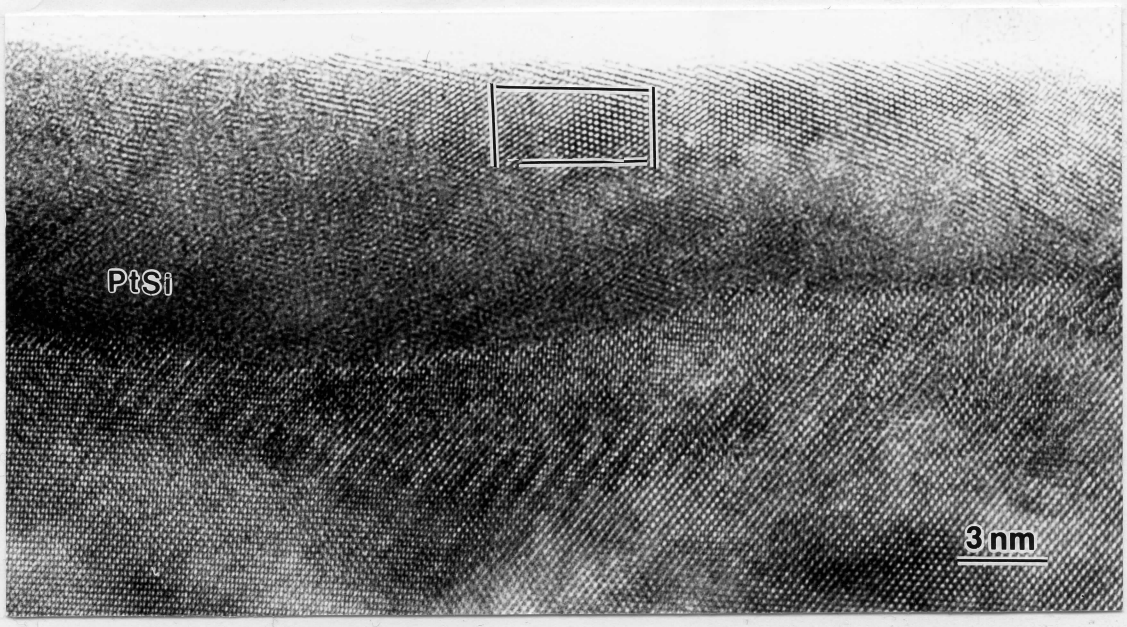
for instance, Muta and Shinoda [Muta 1972]. Muta observed the simultaneous growth of Pt_2Si and PtSi in the presence of residual Pt. Wittmer attributed the discrepancy in D_0 values to the presence of 'contaminations' in samples mentioned by the other authors. By comparing the results of these authors with our observations for samples with and without interfacial oxide layer, we can make the hypothesis that the slowing down of the Pt-Si reaction speed in Muta's samples could be due to the presence of a thin interfacial oxide layer.

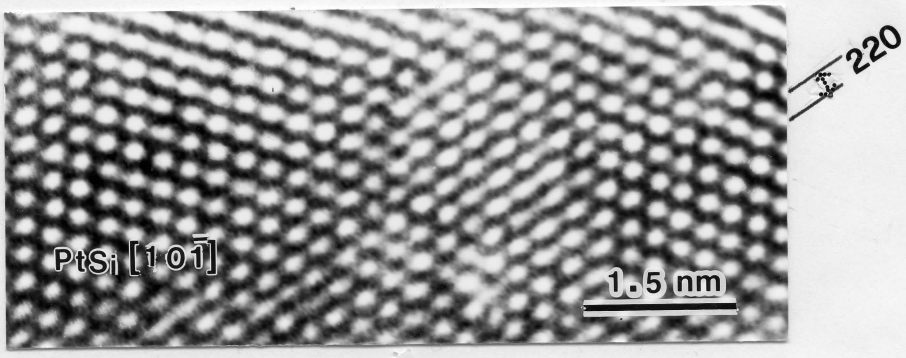
From this observations we can conclude that Majni's and Tsaur's models are valid only for oxide-free samples. If an oxide barrier is present, even as thin as 1.3 nm, the Pt - Si reaction occurs, but following a path that depends also on the density and diameter of the oxide pinholes that control the Pt supply.

IV.2.2 Platinum silicide films annealed at intermediate temperatures

We consider as intermediate temperature the range between 350 - 550 °C. Good crystallographic stability and electrical performance are obtained with films annealed in this range of temperatures, even for samples with a 2.2 nm-thick interfacial oxide layer. These films are described below.

Morphologically, all samples are similar: grains are shaped as polyhedrons which show an increasing average grain size from 20 nm at 350 °C to 40 nm at 550 °C, as we can see in planar-view images of the figures IV.8, 9, and 10 for samples X, Y and Z, respectively. These films, annealed at 550 °C, are continuous, polycrystalline and epitaxial. They represent the morphology obtained over all the annealing temperature range (350 - 550 °C). Crystallographically, as we observed in the ED patterns, above 350 °C the PtSi phase is present in all samples and $Pt_{12}Si_5$ has disappeared. The situation is quite stable up to 550 °C:





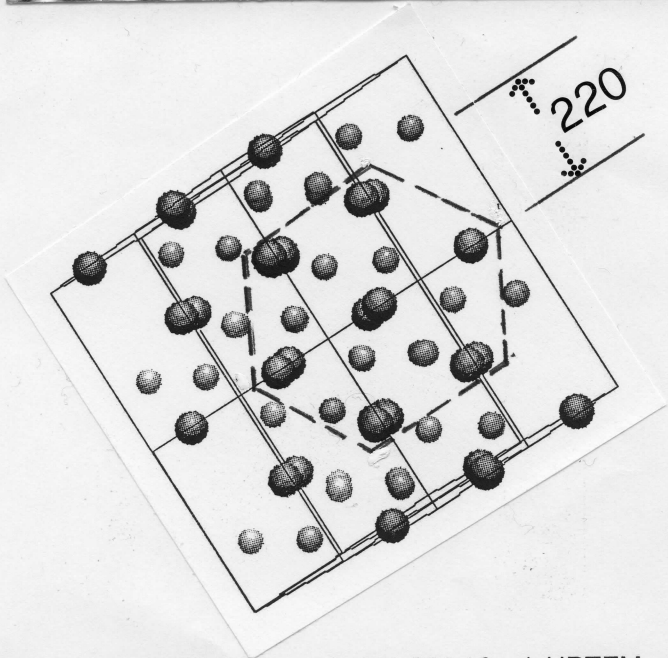
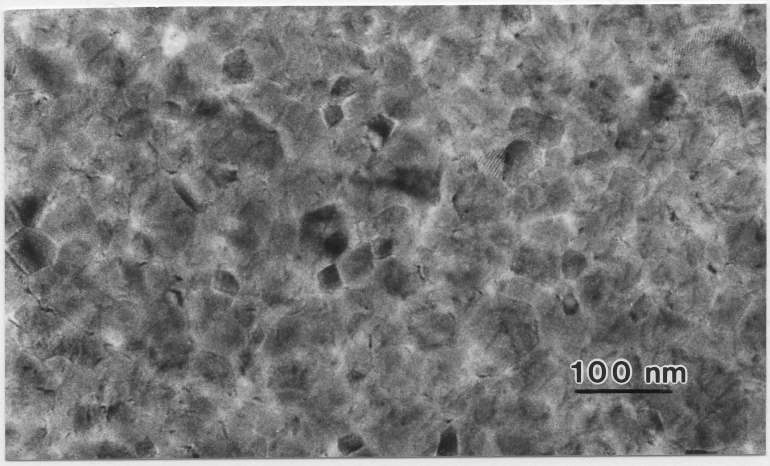


Fig. IV.8: TEM images of sample X annealed at 550 °C. a) HRTEM cross-sectional image, general view. b) Detail of image a), showing a PtSi[1,0,-1] oriented grain. c) Projection of the PtSi structure in the [001] zone axis.



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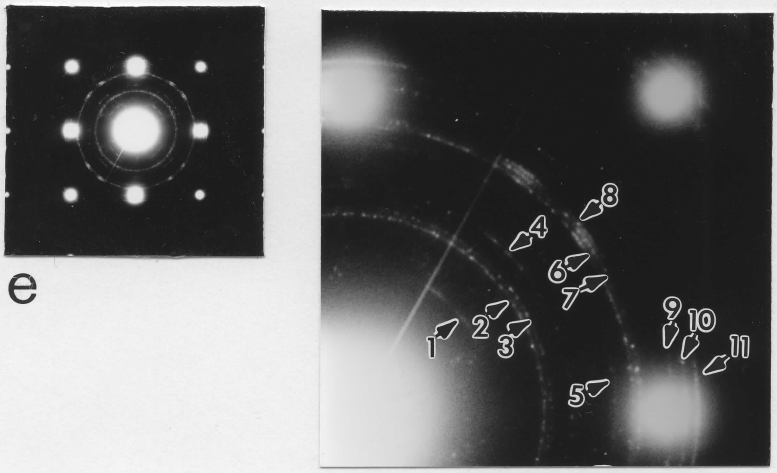
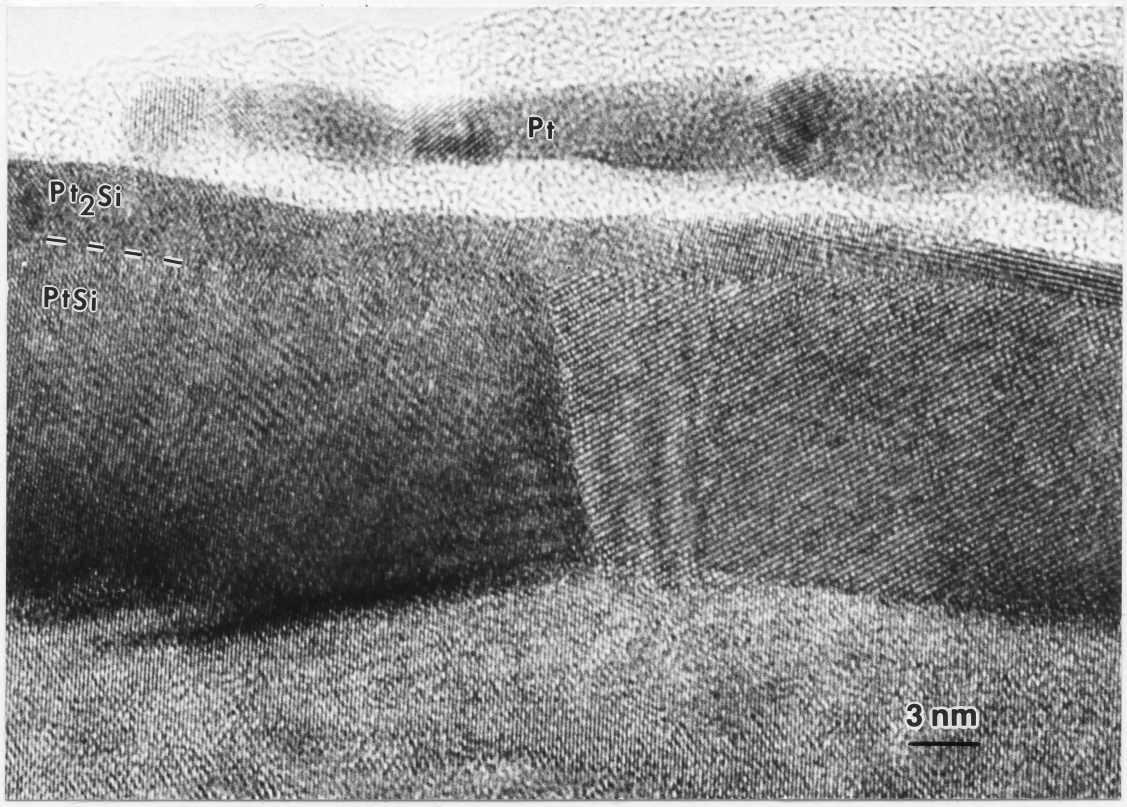
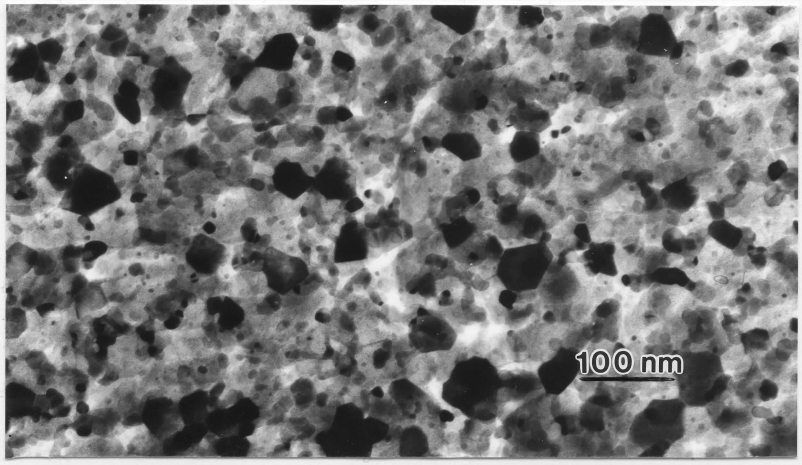


e

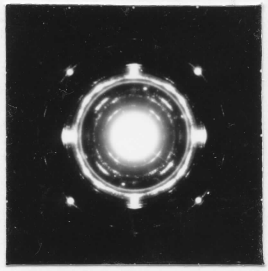
Fig. IV.8 (cont.): d) Planar-view image of sample X (oxide-free) annealed at 550 °C; e) Corresponding ED pattern, showing a general view at left and a detail at right. All arrows indicate the PtSi phase.



a



b



c

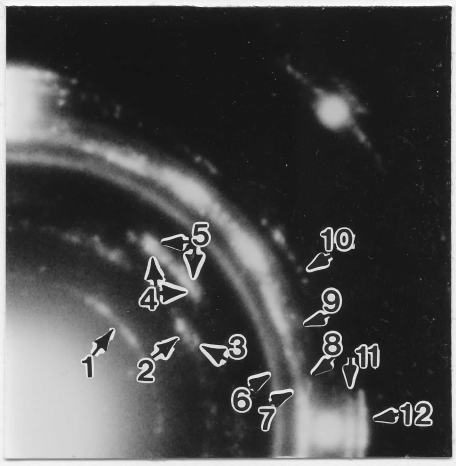
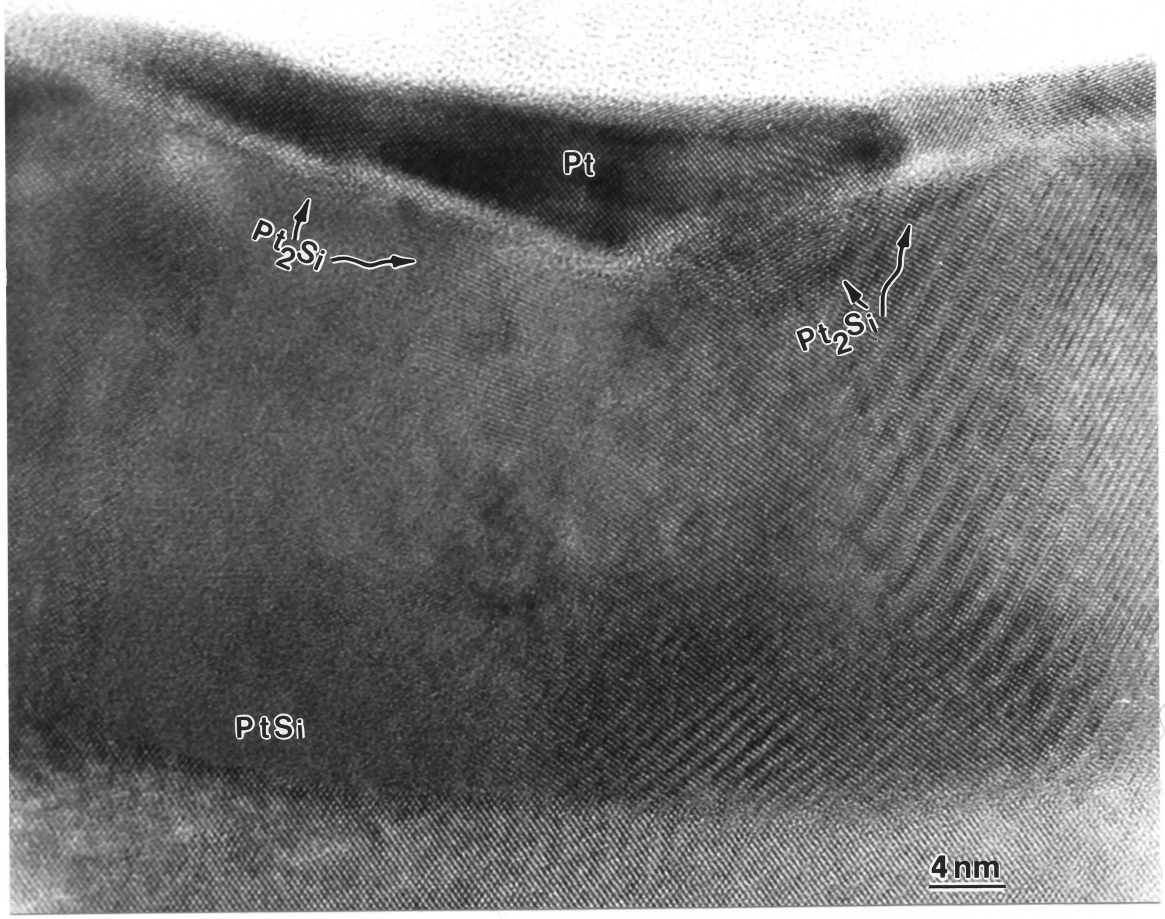
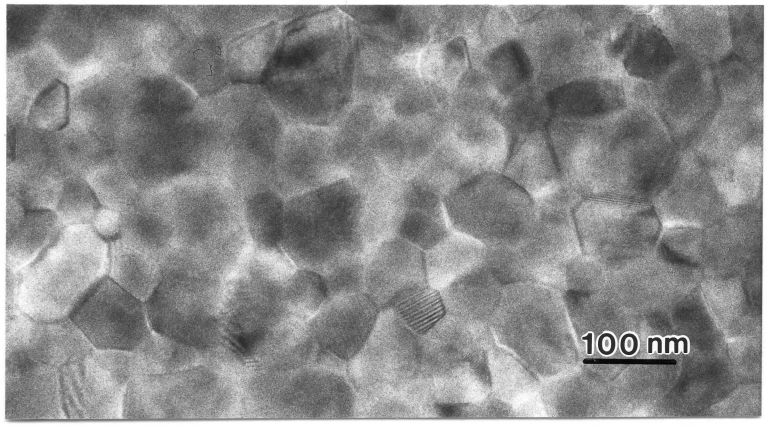


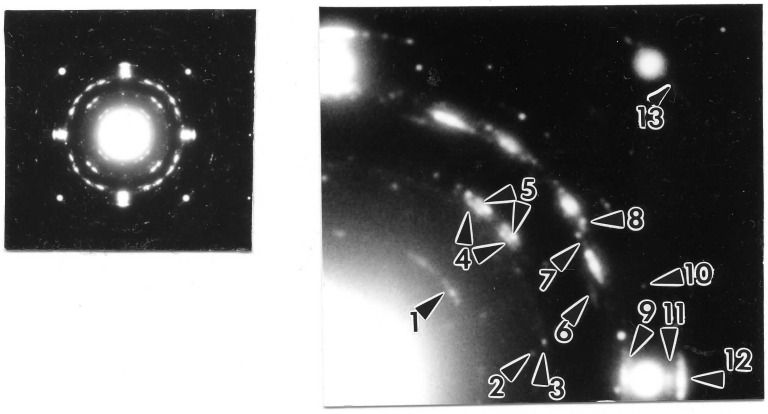
Fig. IV.9: TEM images of sample Y (with 1.3 nm-thick interfacial oxide) annealed at 550 °C. a) HRTEM cross-sectional image. b) Planar-view image. c) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-4-5-7-8-9-10-11-12: PtSi phase; 2-3: Pt_2Si phase; 6: unreacted Pt.



a



b



c

Fig. IV.10: TEM images of sample Z annealed at 550 °C. a) HRTEM cross-sectional image. b) Planar-view image. c) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-4-5-6-7-8-9-10-11-12: PtSi phase; 2-3: Pt_2Si phase; 13: unreacted Pt.

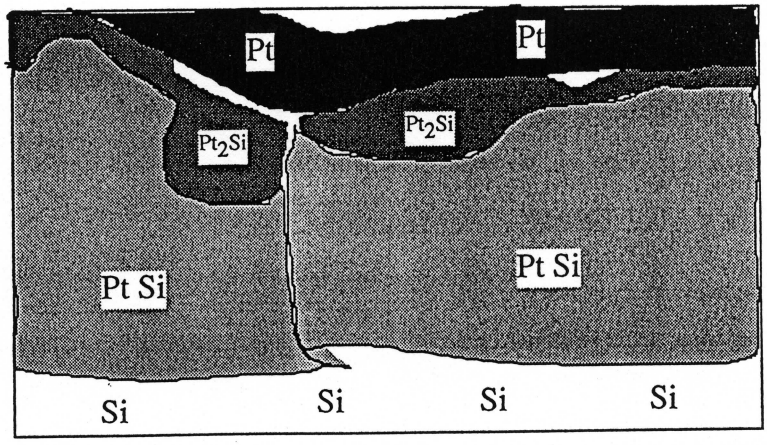
- Sample X, the oxide-free sample, shows the PtSi phase only, formed by textured grains (Figs. IV.8.d and e);

- Samples Y and Z, with different interfacial oxide layer thickness, show the Pt_2Si and PtSi phases, but with a different degree of order: sample Y shows a polycrystalline Pt_2Si phase and PtSi with an long-range crystallographic order increasing (from polycrystalline to polycrystalline with some epitaxy; see figs. IV.9.b and c); sample Z, instead, shows polycrystallinity for both phases with some degree of epitaxy (Figs. IV.10.b and c).

Figure IV.8.a, 9.a and 10.a shows cross-sectional images of the three samples annealed at 550 °C. Because films annealed in the temperature range between 350 and 550 °C are structurally similar, we show only the measurements of the sample annealed at 550 °C as a typical example.

Oxide-free samples (sample X) show a continuous, single phase silicide film (Fig. IV.8.a). It is constituted only by PtSi grains that are formed by sub-grains in different orientations. In Fig. IV.8, the sub-grain at the top of the silicide layer is in PtSi [0,0,1] zone axis, that is parallel to Si[110] direction (see the projected image of Si structure besides the detail of Fig. IV.8.a), as previously mentioned by Ghozlene et al. [Ghozlene 1978]. The bottom part of the layer next to the silicide/Si interface does not show a defined orientation, but PtSi atomic planes in different directions. The silicide/Si interface is quite smooth and some grain facets parallel to Si(111) planes start to form, still at the atomic level.

550 °C-annealed silicide films with a 1.3 nm-thick interfacial oxide layer (Fig. IV.9.a) are structurally similar to those with a 2.2 nm-thick oxide in this temperature range (Fig. IV.10.a). The silicide film is continuous, formed by PtSi grains and a Pt_2Si sub-layer on top. PtSi grains are constituted by sub-grains, i.e., PtSi in different crystallographic orientations. The Pt_2Si sub-layer is found at the top, in contact with



Schematic representation of Fig. IV.10.a

PtSi grains and with the remaining unreacted Pt through the oxide pinholes. The narrow strip formed by the Pt_2Si phase is almost continuous and does not follow the PtSi grains division. The silicide/silicon interface is flat. Some unreacted Pt is still seen but this layer is discontinuous for sample Y (Fig. IV.9.a) and continuous for sample Z (Fig. IV.10.a). A schematic representation of Fig. IV.10.a is shown below, where we can see the continuity between the PtSi grains, capped by a Pt_2Si layer, also continuous. White regions between the Pt_2Si layer and the unreacted Pt correspond to the interfacial oxide.

In this range of temperature silicide films, even with 2.2 nm-thick interfacial native oxide layer, reach a dynamic stability and present the desired morphological, crystallographic and structural characteristics for practical applications.

From our observations we verify that the evolutions of the oxide-free and the two types of silicide films with interfacial oxide layers are quite similar between 350 and 550 °C. Slight differences can be observed, concerning:

- the silicide/Si interface: for the three samples, it is flat, but in the oxide-free case, it is in a more advanced stage than for the other two, showing the formation of facets at the atomic level;

- the unreacted Pt layer: for samples without interfacial oxide, all Pt has reacted (already at 250 °C) to form a continuous and homogeneous PtSi film; for samples with interfacial oxide, the unreacted Pt layer is still present and it is even continuous, for 2.2 nm-thick oxide. The low rate of Pt supply to the silicide layer, in this case, allows us to find the Pt_2Si sub-layer at the top of the silicide layer, in contact with the unreacted Pt through pinholes.

For samples with interfacial oxide, a sort of "dynamic equilibrium" is reached: the reaction speeds at the PtSi / Pt_2Si and Pt_2Si /Pt interfaces appear similar and the PtSi grain distribution as well as the Pt_2Si layer thickness remain almost unchanged over the temperature range mentioned above. As we will describe in Chapter V, the best electrical performance for these films is obtained with this range of annealing temperatures. Silicide films with an interfacial silicon oxide layer which have good transport properties are typically formed by multi-domain polycrystalline PtSi grains, capped by a Pt_2Si narrow strip. Even if the electrical performance decreases for annealing temperatures above 550 °C (as we will see later), the partially etched oxide samples keep this "dynamic equilibrium" up to at least 700 °C, that is the highest temperature predicted by the phase diagram [Massalski 1986] for the existence of the α-Pt_2Si phase and is also the highest temperature at which we observed it.

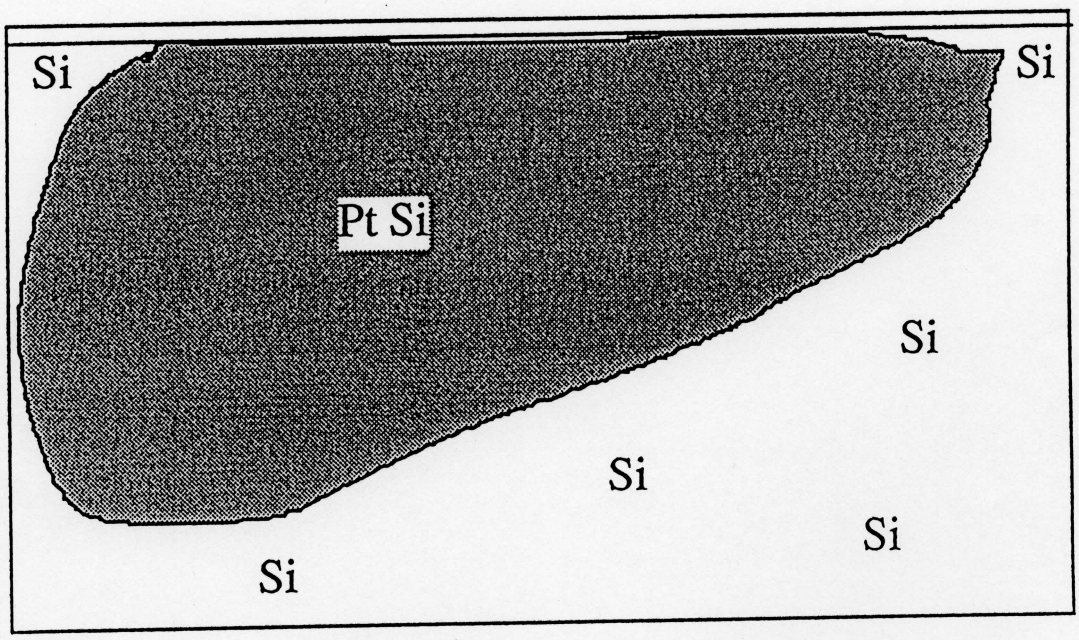
IV.2.3 Platinum silicide films annealed at high temperature

The thermal annealing of our samples was performed at temperatures above the stability range for platinum silicide on Si[100] in order to observe silicide transformations up to the vicinity of the lowest platinum silicide eutectic point, at 830 °C [Massalski 1986]. Temperatures employed were 600, 650, 700, 750 and 800 °C. Atoms migrate away from the thin grains to the large ones generating a film discontinuity. The evolution as a function of the annealing temperature is different for the three kind of samples (oxide-free, 1.3 nm- and 2.2 nm-thick interfacial oxide films), due to the existence, in samples with interfacial oxide layer, of a continuous Pt_2Si layer at the silicide/SiO_2 interface. The existence and characteristics of this Pt_2Si layer depend, once more, on the oxide thickness and pinhole density and diameter.

For oxide-free samples, the atomic-scale facets already seen at 550 °C become more and more pronounced at 600 °C. At the same time, larger grains started to develop while consuming their neighbors that become thinner. At 600 °C, these thinner grains have already lost more than one-half of their original thickness. This process continues until the complete consumption of the small grains leading to film discontinuity, which is already observed at 650 °C and enhanced at 700 °C. At this temperature only very large grains separated by large voids are observed, as we can see in the cross-sectional image (Fig. IV.11.a). In the detail of the cross-sectional image (Fig. IV.11.b) we can observe that this particular grain is oriented with PtSi(002) planes nearly parallel to (220) planes of the substrate.

While developing facets (parallel to the Si(111) direction at the beginning but they can assume another preferential direction during the growth) the PtSi grains re-order themselves until they reach the monocrystallinity. Isolated PtSi grains have roughly a triangular shape, they are monocrystalline and show an epitaxial relationship with the substrate. The Si lattice recrystallizes into the space newly opened between

grains, progressing towards the substrate surface. We also observed Si recrystallization at the silicide/Si interface, where Si is often disordered in the early stages of the Pt-Si reaction at low temperatures. This is due to the formation of the initial amorphous mix between Pt and Si: the disordered region extends for a few monolayers in the substrate. The Si recrystallization is commonly observed from 500 - 550 °C ([Csepregi 1975]; [Csepregi 1976]). We can see clearly this phenomenon in the example of Fig. IV.12, where an isolated grain is surrounded by recrystallized Si. PtSi has also recrystallized. We can suppose that Si recrystallization establishes an epitaxial correlation with PtSi and forces PtSi recrystallization. A schematic representation of Fig. IV.12 is shown below:



Schematic representation of Fig. IV.12

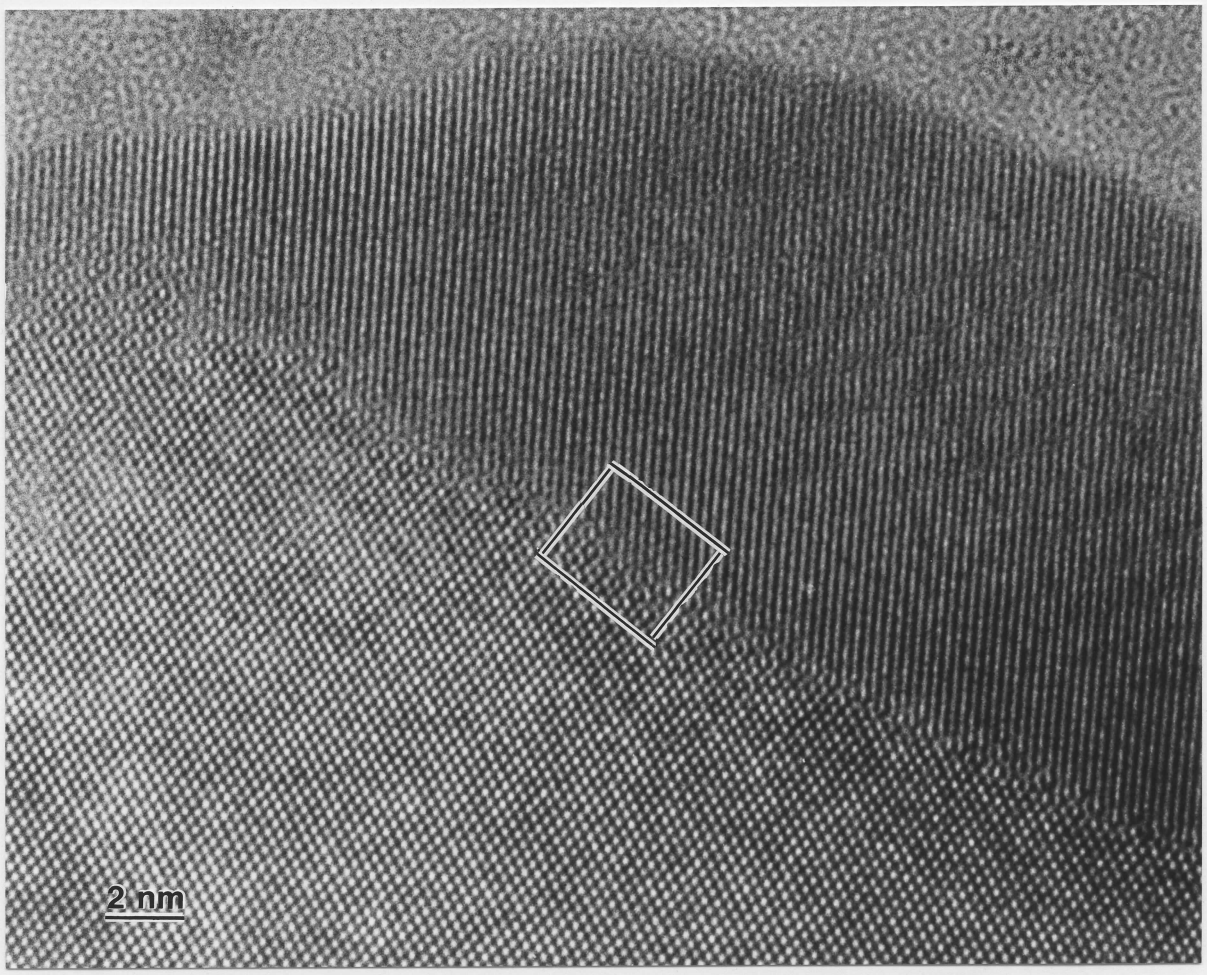
The planar-view micrograph confirms the discontinuity observed by cross-sectional image (Fig. IV.11c). The ED pattern (Fig.IV.11d) shows that the only silicide phase present is PtSi.

For an 1.3 nm-thick interfacial oxide, the film characteristics found for samples annealed at intermediate temperatures (350 - 550 °C) remains stable up to 600 °C at least. The silicide/silicon interface is still flat and lateral facets parallel to Si(111) (trend to the epitaxy) are observed over a few atomic planes. We no longer find unreacted Pt. The narrow polycrystalline Pt_2Si sub-layer detected at the top of the silicide layer for this sample is similar to that observed for the sample annealed at intermediate temperatures. At 700 °C an interesting phenomenon can be observed (Fig. IV.13.a): although facets progress, separating PtSi grains, the continuity of the film is guaranteed by the narrow Pt_2Si sub-layer which does not follow the same process and remains unchanged. The recrystallized Si lattice takes place between PtSi grains. We show below a schematic representation of Fig. IV.13.a:

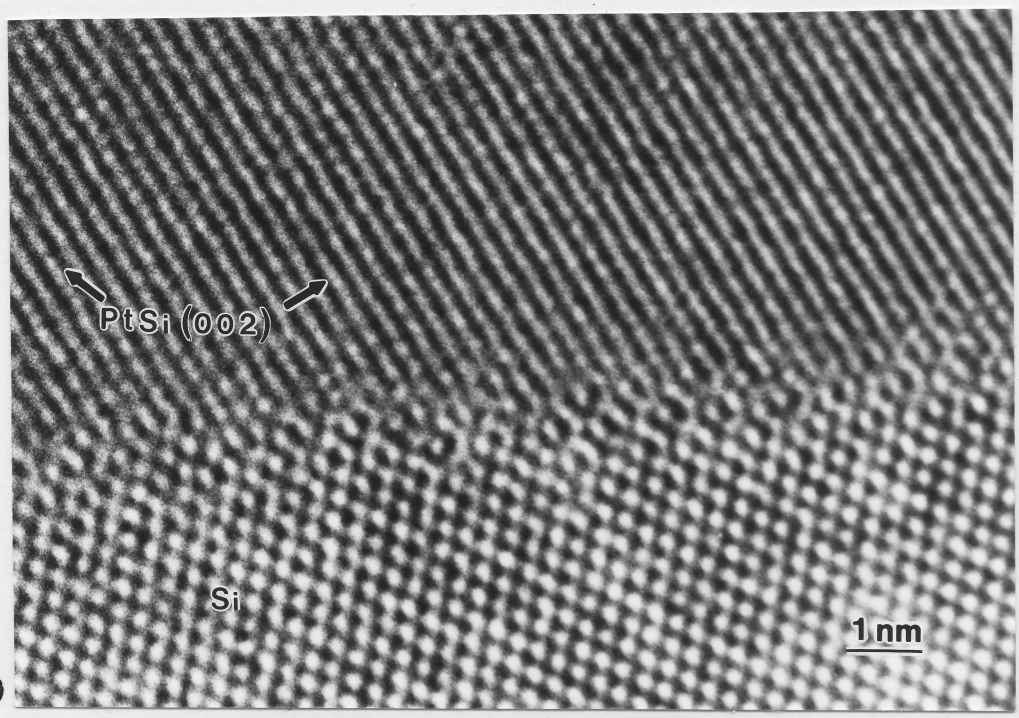
A detail of this continuous and unchanged Pt_2Si sub-layer as well as of the Pt_2Si/PtSi interface at 700 °C is shown in Fig. IV.13.b at higher magnification. Above 700 °C, the phase diagram predicts the disappearance of the α-Pt_2Si phase and, in fact, the Pt_2Si sub-layer is no longer observed at 750 °C. At 800 °C, grains are completely separated.

Planar-view images confirm that layer continuity is observed up to at least 700 °C (Fig. IV.13c). PtSi grains are shaped as polyhedrons, with an average grain size of about 100 nm. The ED pattern (Fig. IV.13d) shows rings and spots (polycrystalline with some epitaxy) for the PtSi phase. Pt_2Si phase is polycrystalline, characterized by rings. At 800 °C, however, the films are discontinuous and only epitaxial PtSi is found.

In the case of the 2.2 nm-oxide interfacial layer the tendency to film discontinuity is observed above 600 °C. In planar-view images, one can observe an increasing density of isolated platinum silicide agglomerates, both large and small. We found two maxima in the grain size distribution rather than one, at 40 - 60 nm and at 100 - 120 nm.

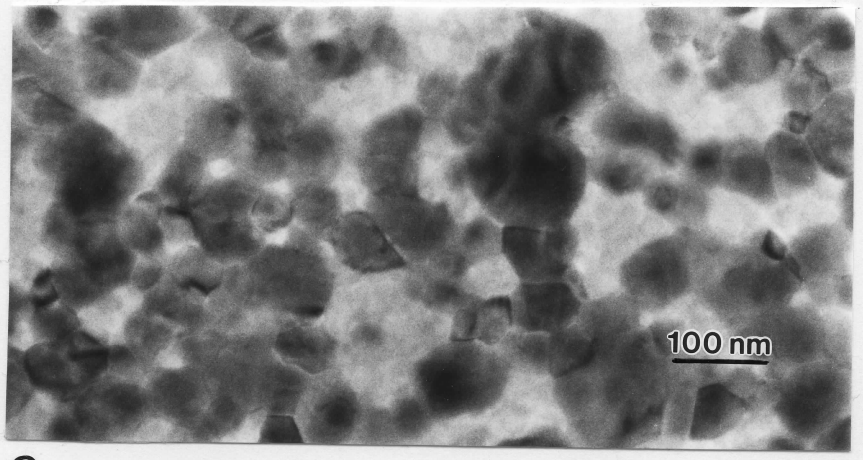


a

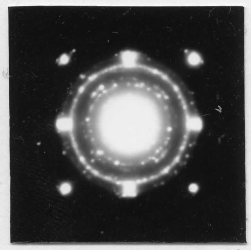


b

Fig. IV.11: TEM images of sample X annealed at 700 °C. a) HRTEM cross-sectional image, showing a partially isolated grain formed by PtSi(002) planes. b) Detail of the PtSi/Si interface.



c



d

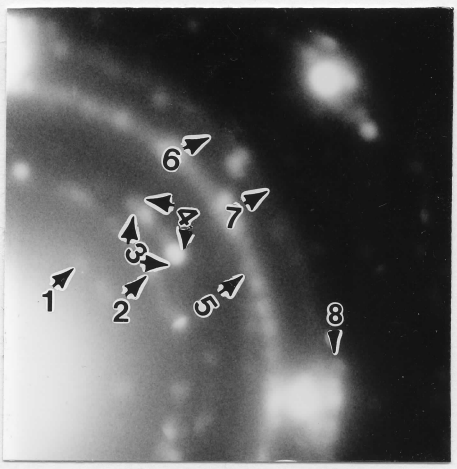
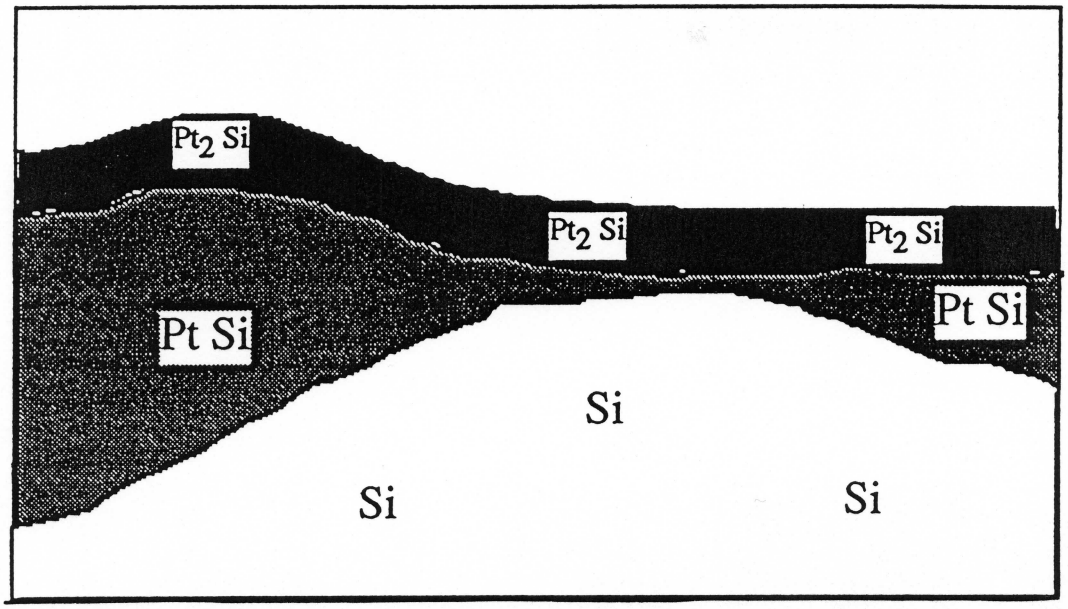


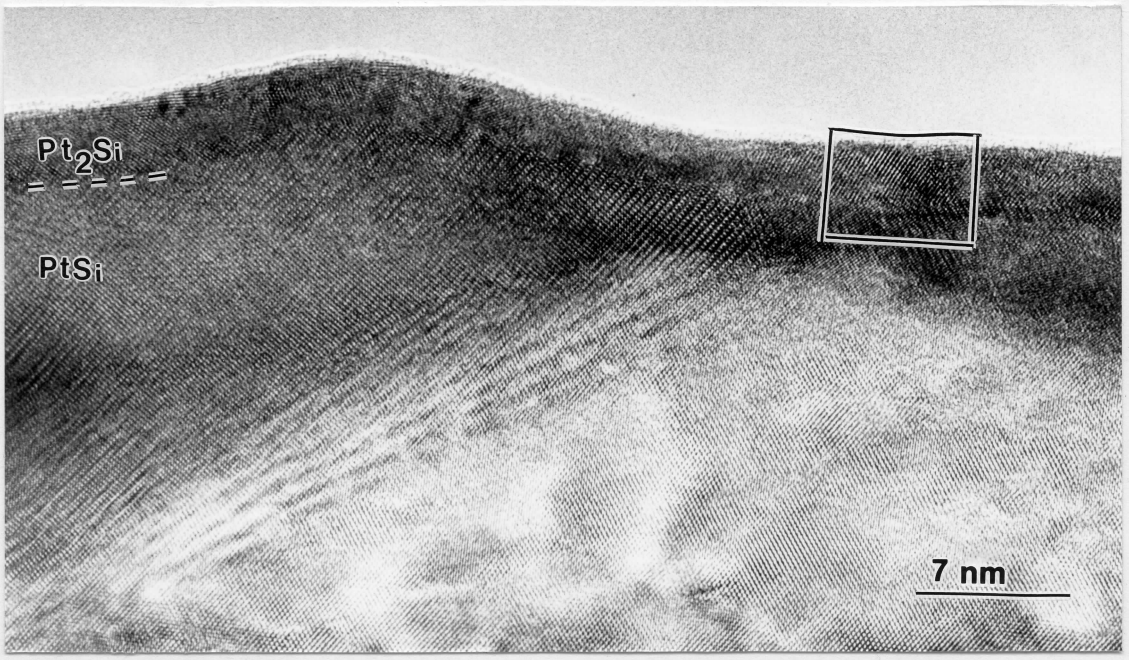
Fig. IV.11 (cont.): c) Planar-view image; d) ED pattern, showing a general view at left and a detail at right. All arrows (1-8) indicate rings and spots diffracted by the PtSi phase.

Fig. IV.12: HRTEM image of an isolated grain (oxide-free sample annealed at 700 °C), showing facets and surrounded by the recrystallized Si. This PtSi grain is monocrystalline.

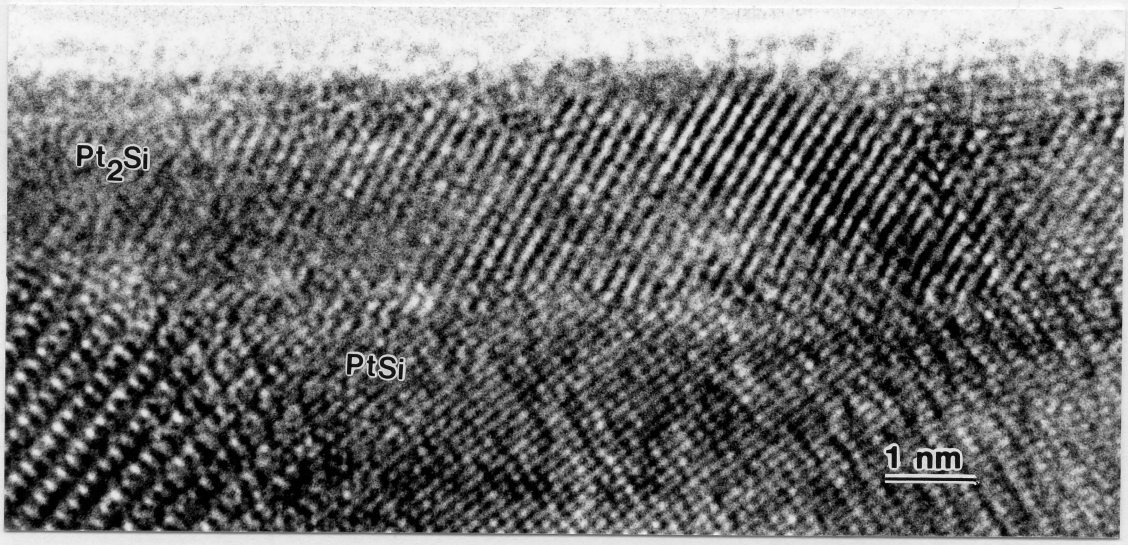


Schematic representation of Fig. IV13.a

At 700 °C, polyhedrons can still be seen, but separated in groups (Fig. IV.14b). This distribution transforms into completely isolated large and small round agglomerates at 800 °C (planar-view, Fig. IV.16a). Crystallographically, the trend is towards epitaxial grains. At 700 °C, the ED pattern (Fig. IV.14c) of the silicide film is constituted mostly by PtSi spots or spots forming rings, indicating that grains are textured. We detected only three weak rings formed by small spots belonging to the Pt_2Si phase ((002) and (110)). At 800 °C, there is no polycrystalline PtSi nor epitaxial Pt_2Si: only epitaxial, isolated PtSi grains remain. Larger grains are [201] oriented and smaller grains are [1,-1,-2] oriented, corresponding to the (220) and (201) directions (ED patterns, Fig. IV.16b).

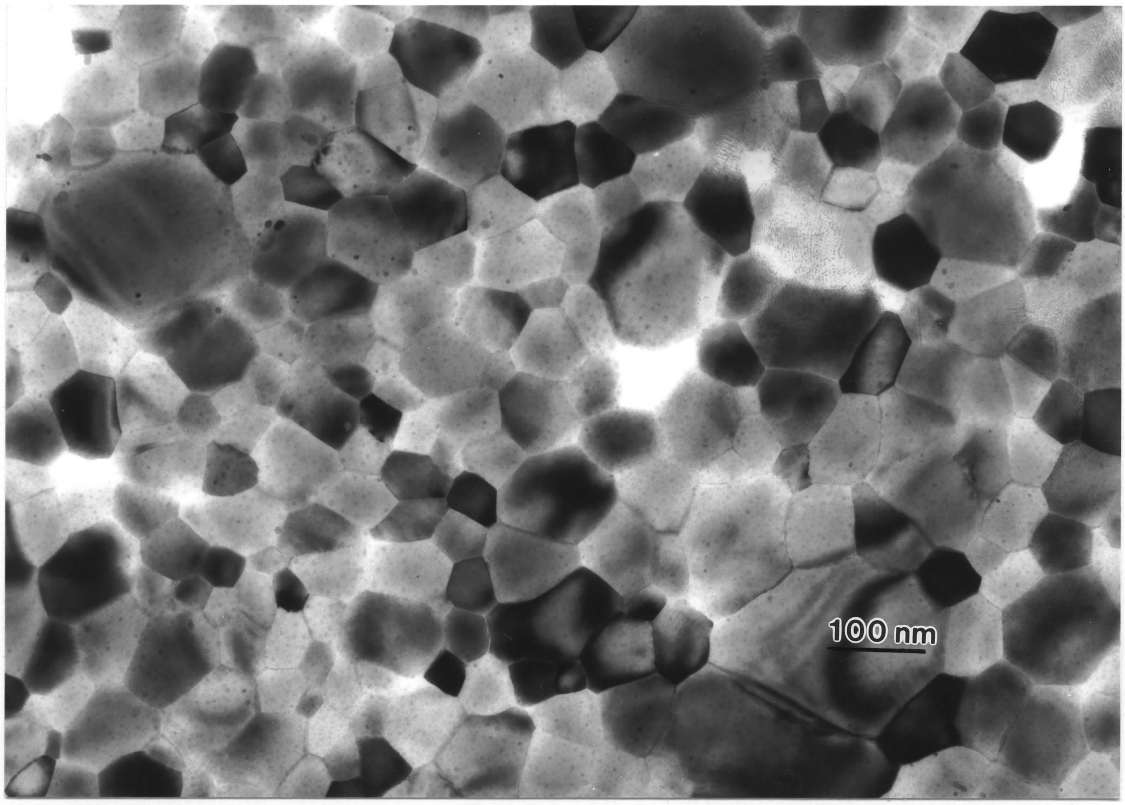


a

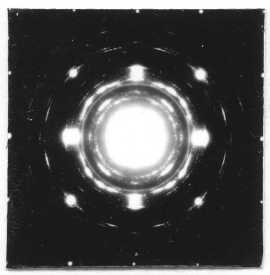


b

Fig. IV.13: TEM images of sample Y (with 1.3 nm-thick interfacial oxide) annealed at 700 °C. a) HRTEM cross-sectional image, showing partially isolated PtSi grains capped by a continuous Pt_2Si layer. b) Detail of the polycrystalline and continuous Pt_2Si layer.



c



d

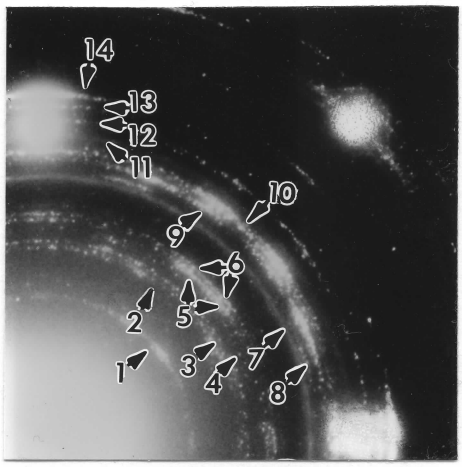
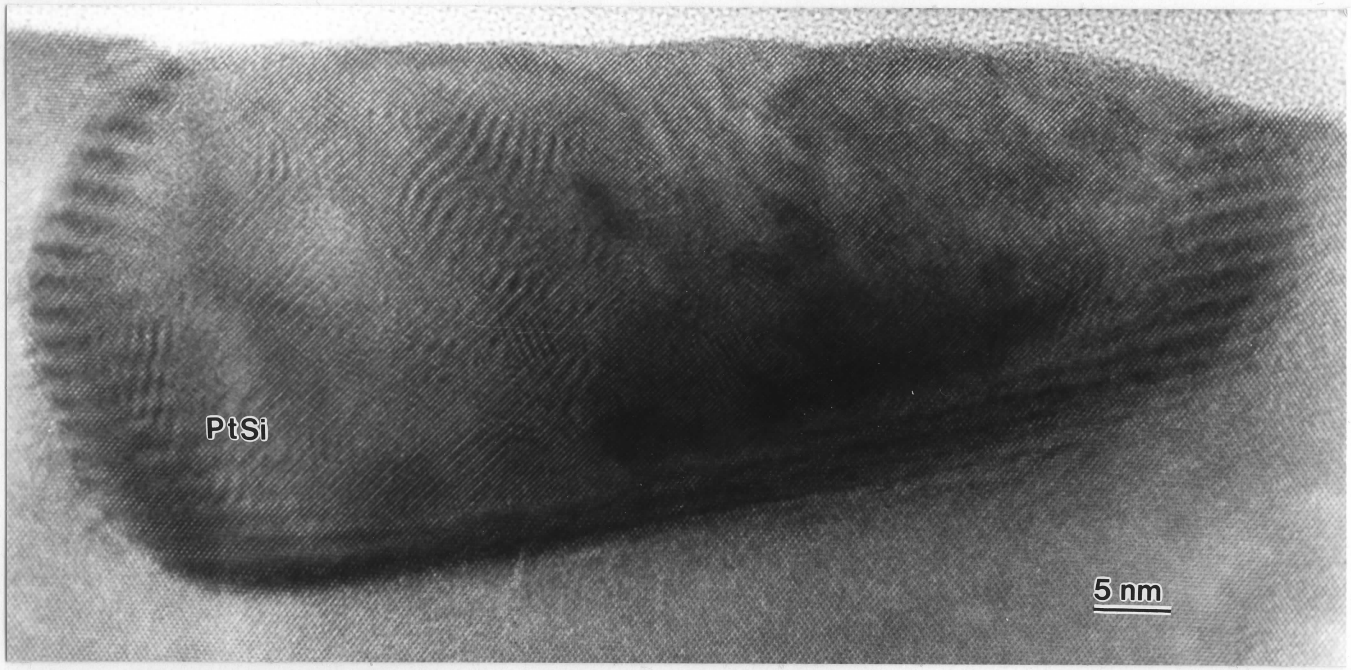
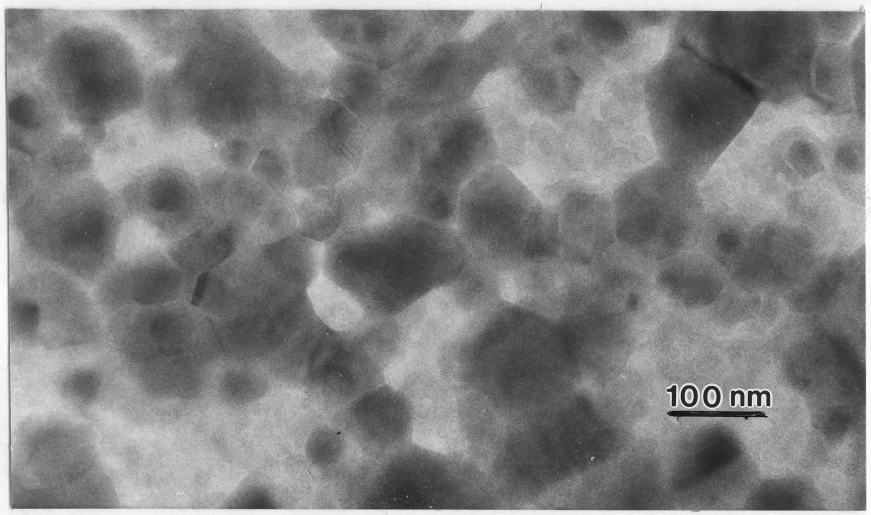


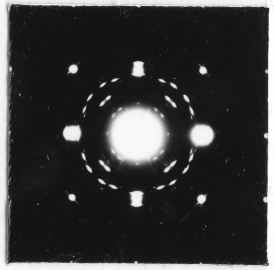
Fig. IV.13 (cont): c) Planar-view image; d) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-2-5-6-7-8-9-10-11-12-13-14: PtSi phase; 3-4: Pt_2Si phase.

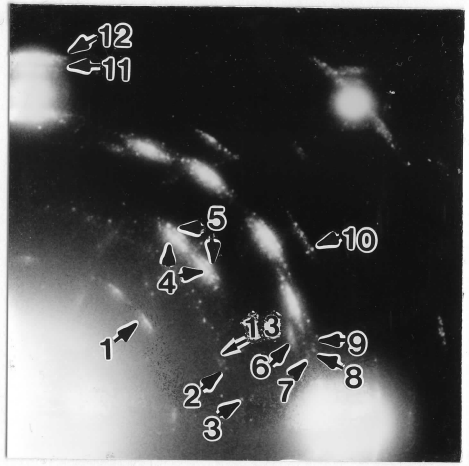


a



b





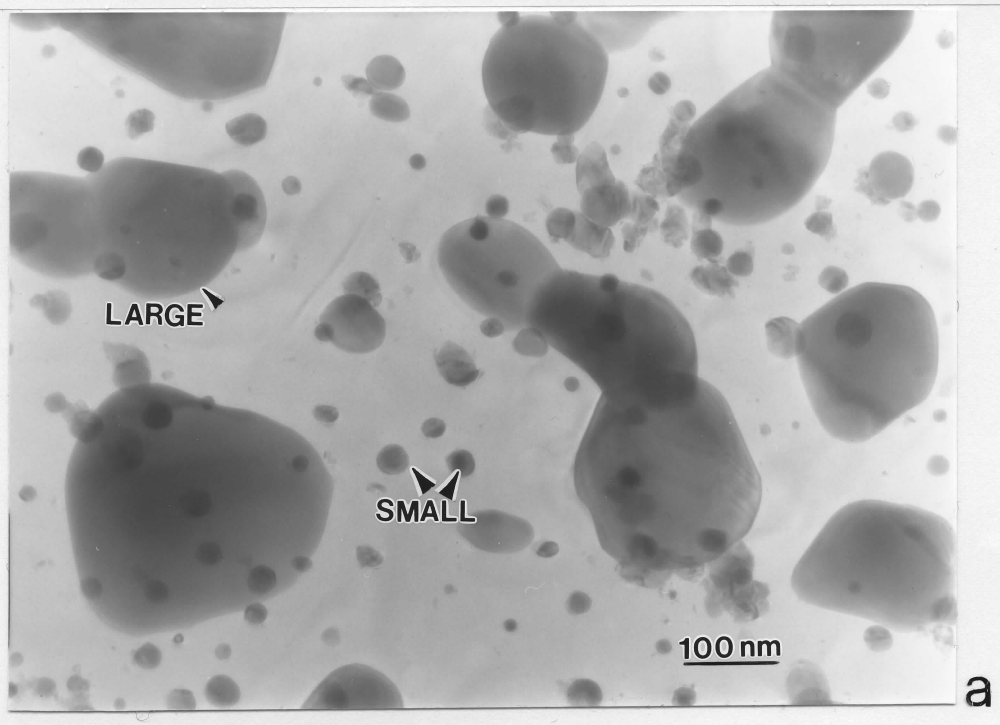
c

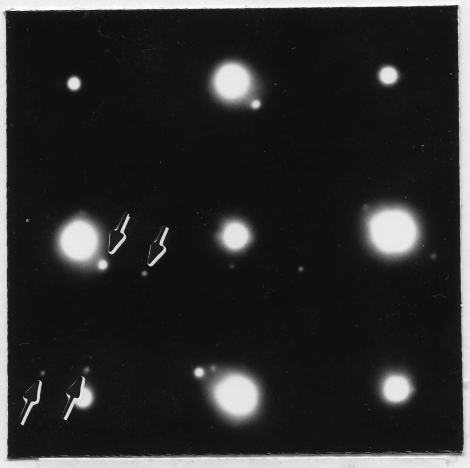
Fig. IV.14: TEM images of sample Z annealed at 700 °C. a) HRTEM cross-sectional image, showing a PtSi isolated grain. b) Planar-view image; c) ED pattern, showing a general view at left and a detail at right. Arrows indicate: 1-2-4-5-6-7-8-9-10-11-12: PtSi phase; 3-13: Pt_2Si phase.

Cross-sectional observations confirm the beginning of the transformation at 600 °C. As in the previous cases, 'multi-domain' silicide grains re-order in to 'single-domain' PtSi grains, with different sizes, showing facets and an epitaxial relationship with the substrate. The growth of these facets disconnects the grains, leading to film discontinuity. In Fig. IV.14a we can see an isolated PtSi grain, without Pt_2Si in the upper part. In fact, the Pt_2Si is no longer continuous at the upper part of the silicide layer. It exists only in regions in contact with unreacted Pt agglomerates. The residual Pt_2Si sub-layer can still be seen at the top of isolated PtSi grains or even alone, in the absence of PtSi grains. The remaining unreacted Pt coalesces to form islands around the upper part of each oxide pinhole at 600 °C, in agreement with the observations of Abelson et al. [Abelson 1988]. Islands of Pt between the SiO_2 pinholes are still visible at 700 °C, but they disappear below 800 °C. As we see no evidence of a Pt-SiO_2 reaction (like changes in SiO_2 thickness or at Pt/SiO_2 interface) even at high temperatures, in agreement with [Abelson 1988] and [Liehr 1985], we conclude that the entire Pt film has reacted with the substrate at 800 °C and the reaction Pt-Si has occurred through the oxide pinholes until full consumption of all the available Pt.

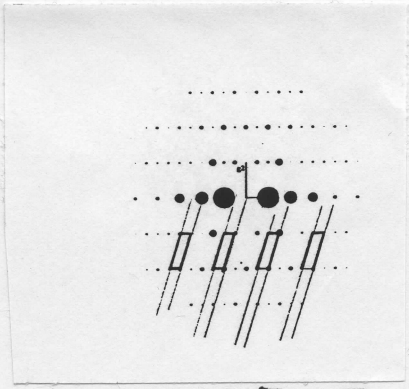
Although discontinuous, the Pt_2Si agglomerates can be found, up to 700 °C, as a connection between PtSi grains and residual Pt agglomerates passing through oxide pinholes. In other cases, it forms an interface directly with Si, without an intermediate PtSi sub-grain. Figure IV.15 shows precisely this situation. Pt_2Si forms an interface with Si at 10 nm below the substrate surface and cross on the oxide pinhole. At this temperature, however, Si diffuses fast enough to reach the upper part of the pinhole and to react with Pt in the Pt agglomerate above the silicon oxide. The silicide agglomerate is constituted by Pt_2Si with atomic planes in the [110] direction and penetrates approximately 2 nm into the Pt agglomerate, above the SiO_2 layer.

Fig. IV.15: A Pt_2Si agglomerate (sample Z annealed at 700 °C) that forms an interface with the Si substrate, cross the oxide pinhole and penetrates 20 Å into the unreacted Pt agglomerate. It is formed by planes in (110) direction.

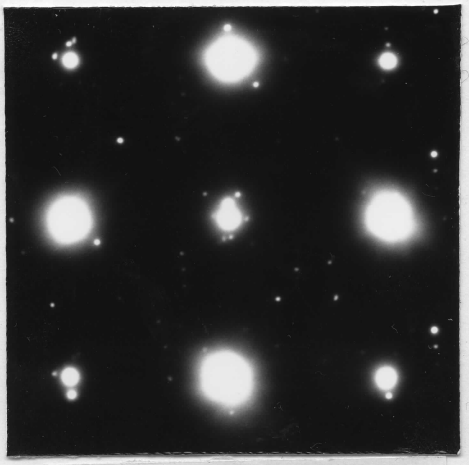




Large Agglomerates



PtSi [201]



b

Small Agglomerates

Fig. IV.16: TEM images of sample Z annealed at 800 °C. a) Planar-view image. b) ED patterns of large agglomerates PtSi[201] oriented (simulated diffraction included) and small agglomerates, in PtSi[1,-1,-2] orientation.

The mechanism that leads to the silicide film discontinuity seems to be similar for the three types of samples: PtSi facets appear, simultaneously to the Si recrystallization at the silicide/silicon interface. We observed the beginning of the Si recrystallization between 500 - 550 °C, in agreement with Csepregi et al. ([Csepregi 1975]; [Csepregi 1976]). This transformation progresses from the bottom of the grain towards the Si surface along the grain boundaries. With increasing of the annealing temperature facets become more pronounced and progressively separate each grain from its neighbors. Some large grains become even larger and deeper by incorporating their neighbors. In this process, the small grains whose atoms migrate to the larger grains become thinner and then disappear. This is clearly the only transformation mechanism present in oxide-free samples. Some evidences of this transformation can be already seen at 550 °C. It progresses up to 700 °C, where PtSi grains are epitaxial and isolated.

For samples with interfacial oxide, however, two mechanisms seems to be in competition: on the one hand there is Pt_2Si formation in the course of the Pt-Si reaction, and its later transformation into PtSi (tendency to keep the continuity); on the other hand, there is the re-ordering of the PtSi leading to a discontinuous, island-type film. If the oxide is thick, the Pt diffusion is limited (the remaining unreacted Pt up to 650 °C is non-negligible) and the PtSi re-ordering becomes faster. This is clearly observed already at 600 °C. Pt diffusion speed through the oxide pinholes towards the silicide film (slowed down by the oxide barrier) to form silicide is not sufficient to compensate for the speed of silicide re-ordering. Once more, the pinholes density and pinholes diameter play an important role in the film evolution. Thus, the PtSi re-ordering predominates and the film becomes discontinuous above 650 °C.

We can observe progressively the depletion and discontinuity of the Pt_2Si layer. The fast increase of PtSi order is showed by the facet formation and by the transformation from multi-domain grains to epitaxial grains in the bulk of silicide grains. The Pt_2Si grain we showed in Fig. IV.15 was not yet depleted at 700 °C perhaps because there was no PtSi between it and the substrate. The existence of

such a mechanism was also predicted by Majni et al. [Majni 1985]. Above 700 °C, residual Pt can still react with silicon, but it forms PtSi directly.

With a thin oxide layer, the unreacted Pt diffuses moderately. The three reaction speeds (the Pt_2Si and PtSi formation and the PtSi re-ordering) remain in equilibrium until the complete consumption of the unreacted Pt, between 650 and 700 °C. The Pt_2Si layer is continuous and homogeneous in thickness up to 700 °C and disappears above this temperature (as predicted by the phase diagram). The remaining contact between PtSi grains becomes smaller and smaller, until the discontinuity sets in, around 750 °C. The temperature where film discontinuity occurs is, in fact, higher for samples with a thin interfacial oxide than for thick interfacial oxide or oxide-free samples. The Pt diffusion controlled by the 1.3 nm-thick interfacial oxide layer is actually beneficial, slowing down the island formation process.

IV.3 Photoelectron microscopy

Photoelectron Microscopy (PEM) analyses confirm the existence of PtSi and Pt_2Si phases in samples with 1.3 nm- and 2.2 nm-thick interfacial native oxide (Y and Z). We obtained images and spectra, simultaneously, from the same regions. Our spectra were obtained with Pt 5p electrons, with a binding energy corresponding to 51.7 eV. 5p electrons in Pt_2Si compound have binding energy of 52.9 eV and in PtSi, 53.4 eV. The binding energy for Pt_2Si and PtSi was observed by Grunthaner et al. [Grunthaner 1982] for 250 °C-annealed 50 nm-thick platinum silicide films analyzed by x-ray photoemission. For Si analysis, we obtained images and spectra in the 98 - 112 eV region using Si 2p electrons.

Figures IV.17 and 18 show PEM spectra obtained for samples Y and Z. The yield corresponds to the emitted photoelectrons excited by photons in the 50 - 60 eV range (Pt 5p electrons) as a function of the annealing temperature.

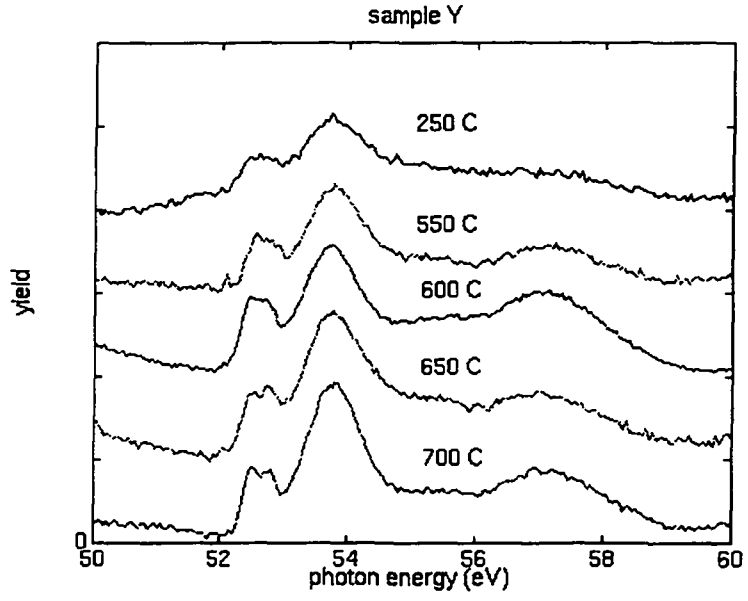


Fig. IV.17 - PEM spectra for sample Y at various annealing temperature, in the 50 - 60 eV energy range.

The background was subtracted from all spectra. The resulting peaks represent, actually, the absorption edge of the incident photons. Detected outcoming electrons have the energy absorbed from photons minus the energy corresponding to the work function. For Pt electrons the work function is 5.3 - 5.5 eV [Ertel 1950]. This gives us a range of 45 - 55 eV in energy for detected photoelectrons.

For both types of samples (with 1.3 nm- and 2.2 nm-thick interfacial oxide) we observe the presence of Pt_2Si and PtSi phases simultaneously up to 700 °C, as seen previously by electron diffraction. However, absorption edges are slightly shifted with

respect to the expected positions and the absorption edge corresponding to the unreacted Pt (51.7 eV) is not clearly visible. It is probably overlapped with that corresponding to Pt_2Si. The photoelectron yield corresponding to the PtSi line (absorption edge at 53.7 eV) increases with the increasing temperature, indicating the quantitative increase of this phase in the sample. This result confirms, over a large observation area, the results previously obtained by TEM over smaller regions.

For elemental Si, the expected binding energy (Si 2p electrons) is 99.4 - 99.8 eV, (depending on the doping) and 100.5 eV for Si in both types of silicide, Pt_2Si and PtSi [Grunthaner 1982] . The work function for Si electrons is 3.95 eV (n-type) [Meyerhof 1947].

Spectra in the photon absorption range of 98 -112 eV (emission of Si 2p electrons) show two absorption edges not well defined, the first one including the edge expected for elemental Si and Si in silicide and the second identified as Si in SiO_2. These spectra do not show any clear correlation between the photoelectron yield and the annealing temperature.

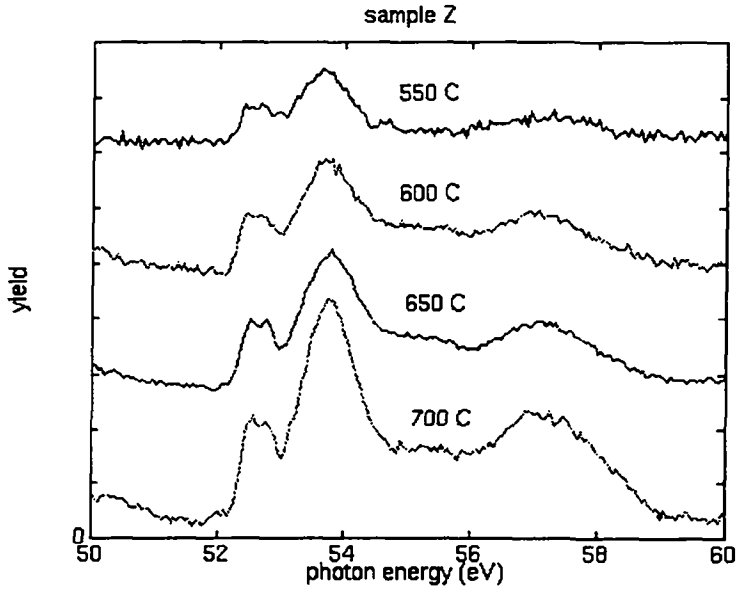


Fig. IV.18 - PEM spectra for sample Z at various annealing temperature, in the 50 - 60 eV energy range.

The image of sample Z annealed at 800 °C (Fig. IV.19) shows clearly an island-type film, in good agreement with TEM analysis. It was obtained by electronic subtraction of the images recorded at an energy slightly higher and slightly lower than that expected for the binding energy of Pt 5p electrons in PtSi, i.e., at 53.8 and 53.1 eV.

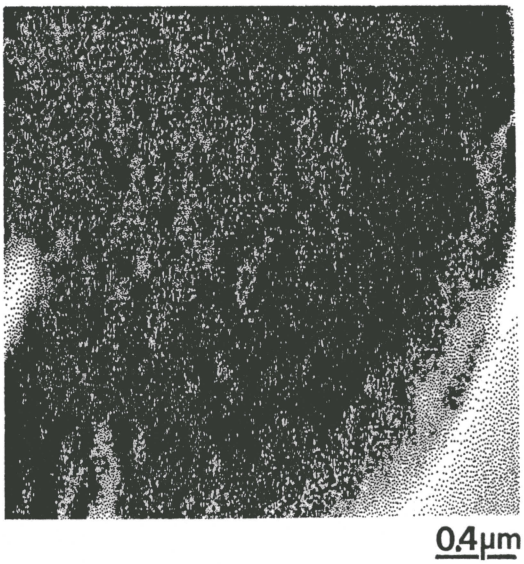


Fig. IV.19 - PEM image of sample Z annealed at 800 °C.

IV.4 Conclusions

In conclusions to this Chapter, we can say that:

- In presence of an interfacial oxide layer, the reactants interdiffuse through the oxide pinholes.

- In the early stages, the Pt - Si reaction follows the expected steps only in oxide-free samples. If an oxide barrier is present, even as thin as 1.3 nm, the reaction also depends on the density and diameter of oxide pinholes.

- After annealing at intermediate temperatures (350 - 550 °C), samples with or without oxide are structurally similar: the silicide layer is constituted by PtSi polycrystalline and epitaxial grains. This layer is continuous and forms a flat interface with the substrate. In this annealing temperature range the difference between silicide films with or without an interfacial oxide layer is the presence of a Pt_2Si sub-layer, at the top of the silicide layer, in contact with the remaining unreacted Pt. It is observable only in samples with an oxide barrier.

- After annealing at high temperatures, the PtSi grains form facets that lead to film discontinuity. In the presence of the Pt_2Si layer, which is not submitted to the same degradation mechanism, the continuity of the silicide layer can be guaranteed up to 700 °C. The Pt flux required to guarantee the continuity of this layer depends on the pinhole density.

In summary, our systematic high-resolution electron microscopy study has eliminated many important points of uncertainty about the formation of silicide on native-oxide-covered silicon. The most important is that it is possible to obtain a continuous film, as required for most applications, even with an interfacial oxide layer, in the form of a combination of epitaxial and non-epitaxial silicide grains obtained in the 350 - 550 °C annealing temperature range. The attempt in promoting epitaxy by increasing the temperature does succeed, but the result is instead a loss of film continuity.

REFERENCES

[Abelson 1988] R. Abelson, K.B. Kim, D.E. Mercer, R. Helms, R. Sinclair and T.W. Sigmon, J. Appl. Phys. **63**(3), 689 (1988).

[Csepregi 1975] L. Csepregi, J.M. Mayer, and T.W. Sigmon, Phys. Lett. **54A**(2), 157, (1975);

[Csepregi 1976] L. Csepregi, E.F. Kennedy, S.S. Lau, J.M. Mayer and T.W. Sigmon, Appl. Phys. Lett. **29** (10), 646, (1976).

[Ertel 1950] A. Ertel, Phys. Rev. **78**, 353 (1950).

[Ghozlene 1978] H.B. Ghozlene, P. Beaufrère, and A. Authier, J. Appl. Phys. **49**(7), 3998 (1978).

[Grunthaner 1982] P.J. Grunthaner, F.J. Grunthaner and A. Madhukar, J. Vac. Sci. Technol., **20**(3), 680 (1982).

[Liehr 1985] M. Liehr, F.K. LeGoues, G.W. Rubloff and P.S. Ho, J. Vac. Sci. Technol. **A3**(3), 983 (1985).

[Majni 1985] G. Majni, M. Costato, F. Panini, and G. Celotti, J. Phys. Chem. Solids **46**(5), 631, (1985).

[Massalski 1986] T.B. Massalski, "Binary Alloy Phase Diagrams", 1st ed., American Soc., p.1909 (1986).

[Meyerhof 1947] W. Meyerhof, Phys. Rev. **71**, 727 (1947).

[Muta 1972] H. Muta and D. Shinoda, J. Appl. Phys. **43**(6), 2913, (1972).

[Ottaviani 1979] G. Ottaviani, J. Vac. Sci. Technol. **16**, 1112 (1979); Thin Solid Films **140**, 3 (1986).

[Stadelmann 1987] P.A. Stadelmann, Ultramicroscopy **21**, 131 (1987).

[Tonner 1989] B.P. Tonner and G.R. Harp, J. Vac. Sci. Technol. **A7**(1), 1, (1989).

[Tonner 1988] B.P. Tonner and G.R. Harp, Rev. Sci. Instrum. **59**(6), 853 (1988).

[Tonner 1990] B.P. Tonner, Nucl. Instr. and Meth. **A291**, 60 (1990).

[Tsaur 1981] B.Y. Tsaur, S.S. Lau, J.W. Mayer and M.-A. Nicolet, Appl. Phys. Lett. **38**(11), 922 (1981)

[Tsui 1990] B-Y. Tsui and M-C. Chen, J. Appl. Phys. **68**(12), 6246 (1990).

[Tu and Mayer 1978] K.N. Tu and J.M. Mayer in "Thin Films - Interdiffusion and Reaction", edited by J.M. Poate, K.N. Tu and J.W. Mayer, Wiley Interscience, New York (1978).

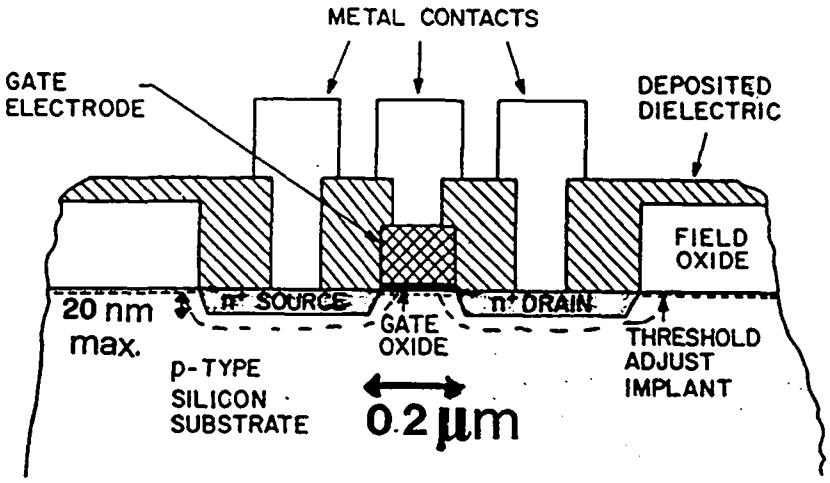
[Wittmer 1983] M. Wittmer, J. Appl. Phys. **54**(9), 5081 (1983).

CHAPTER V

Resistivity Measurements

The resistivity of silicides is a very important parameter when considering them for metallization in integrated circuits. In particular, the low resistivity of platinum silicide makes it very attractive in silicon device technology ([Murarka 1983]; [Sze 1981]). The resistivity of a thin film strongly depends on the steps of the fabrication process. The use of junctions having a depth of approximately 0.1 μm (e.g., in the source and drain areas) and the requirement of using a conductive film with sheet resistance in the order of magnitude of ~ 10 Ω/□ motivated Koenecke et al. [Koenecke 1981] to propose the PtSi as a candidate to make contacts. As the conducting layer have to be thinner, the conductance of the material employed must to be higher. Authors mentioned above demonstrated a method which is able to accomplish the reduction of the current 100 Ω/□ sheet resistance to 10 Ω/ employing PtSi Schottky contacts in the source and drain areas. Platinum silicide belongs to the group VIII metal silicides which have relatively low resistivity with respect to other metal silicide groups. This is thought to be due to the relatively short metal-silicon distances compared to the metal-metal or silicon-silicon distances in the crystalline structure [Murarka 1983].

We show in Fig. V.1 a schematic view of a MOSFET cross-section as an illustration. The reduction of the gate electrode width to 0.2 μm forces the reduction of the source and drain depth to 20 nm, i.e., to a tenth of the gate width. This limitation is imposed by the lateral metal diffusion from the source and drain below the gate. If



gate : 0. 2 µm

n^+ depth: 20 nm

Fig. V.1: Schematic view of a MOSFET cross-section (from [Sze 1985]).

the source and drain are formed by thicker metallic layers, there is the risk of contact between them due to metal diffusion resulting in a device failure.

The resistivity ρ of a film is commonly measured by the four-point probe method [Murarka 1983]. This method gives the resistivity of films as thin as 3.0 nm. The measurement is easy to perform: it consists in sending a current between the two outer probes and measuring simultaneously the voltage between the two inner probes. This technique makes it possible to follow the evolution of the layer resistivity after thermal treatments and to establish the condition for the best electrical performance in relation with the morphological and structural characteristics of the film. Care must be taken to establish a bridge between morphological information obtained by Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), and Electron Diffraction (ED) with the electrical parameters. But the use of this cheap and easy-to-do electrical

measurement will one allow to deduce information about the evolution of the film morphology with heat treatment.

V.1 Experimental procedure

Using the four-point probe method we studied the resistivity as a function of the annealing temperature for the following samples: 20 nm-thick platinum silicide layers with and without interfacial silicon oxide layer; 4 - 5 nm-thick platinum silicide layers with various amounts of plasma damage on the substrate surface; and finally, 2.9 - 3.5 nm-thick films with different plasma etching damage depth. We used a in-line setup, obeing the measurements conditions as described in Chapter III. Samples were 10 x 10 mm squares; the current applied between the two outer probes was 0.3 mA. Measurements were performed at room temperature.

V.2 Platinum Silicide films with interfacial silicon oxide barrier

We studied the resistivity as a function of the annealing temperature for three groups of platinum silicide films characterized by a similar silicide film thickness. This set of samples differs by the interfacial oxide layer thickness which is zero for sample X, (1.3 ± 0.2) nm for sample Y and (2.2 ± 0.3) nm for sample Z. The morphological and crystallographic properties of these samples are discussed in Chapter IV.

We will see below that, for a 250 - 550 °C annealing temperature range, 20 nm-thick platinum silicide films processed in the presence of aresidual oxide layer as thick as 2.2 nm can yield devices with a resistivity as low as 30 μΩcm. The continuity and the

electrical usefulness of the film can be preserved at higher annealing temperature by using process conditions (a thin oxide barrier, for instance) that slow down the Pt - Si reaction and, eventually, island formation.

Figure V.2 shows the resistivity as a function of the annealing temperature. Resistivity values were calculated using thickness values measured directly on HRTEM negatives, as already described in Chapter III. The reference metallic film

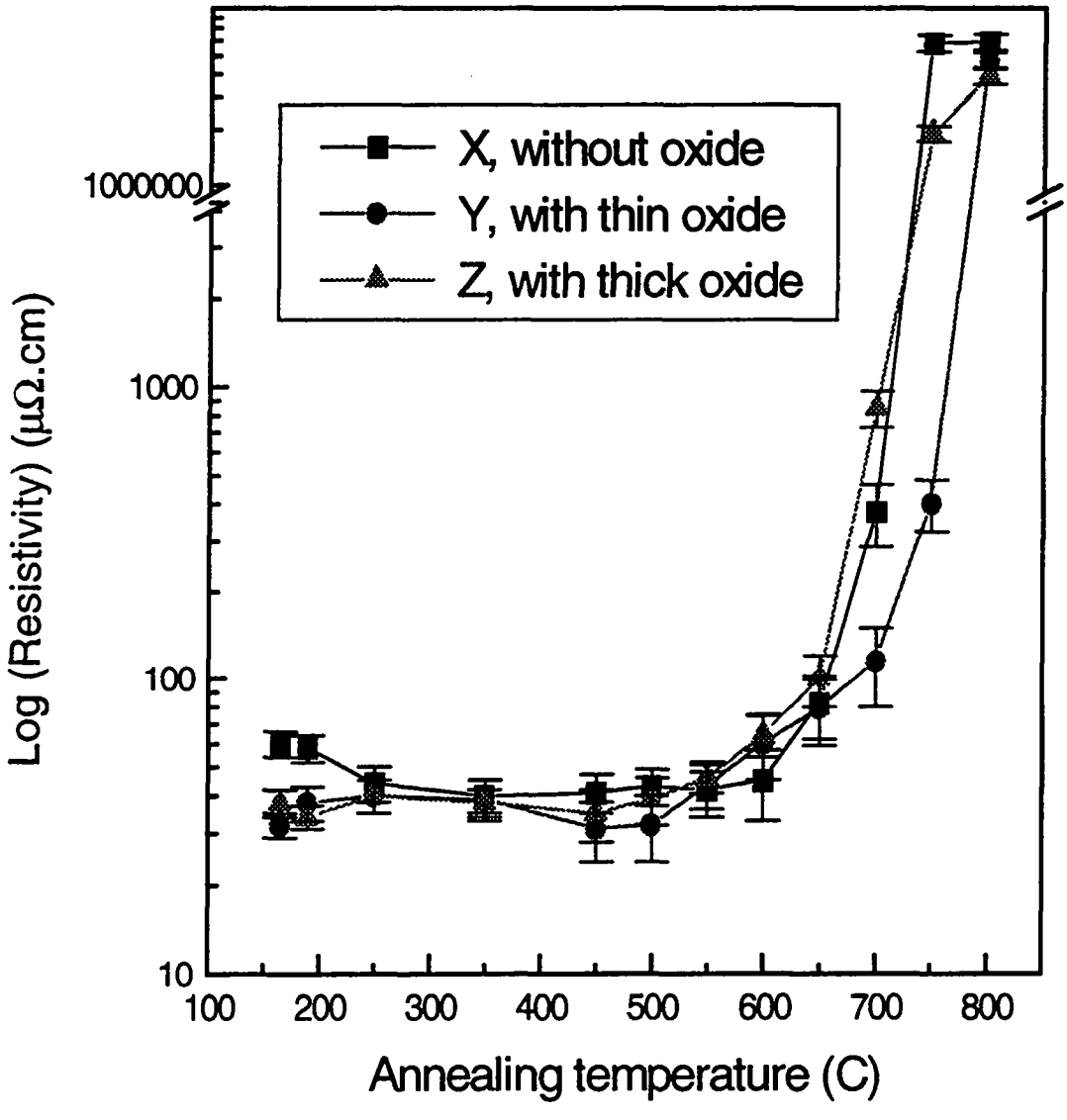


Fig. V.2 - Resistivity as a function of the maximum annealing temperature for 20 nm-thick silicide films: sample X, without interfacial oxide; sample Y, with 1.3 nm-thick interfacial oxide; and sample Z, with 2.2 nm-thick interfacial oxide.

next paragraphs, this difference is related to the temperature in which silicide films become discontinuous.

The different behavior observed for the three samples can be related to the different Pt-Si reaction with and without oxide at low annealing temperatures. These differences are due to the different morphologies of the silicide film which depends on the interfacial oxide thickness (see Chapter IV). Sample X, without oxide, shows a *decreasing resistivity* associated with silicide formation simultaneously to the annealing of defects created during the metallic film deposition on the substrate surface [Murarka 1983] or, eventually, defects generated by the chemical etching. Also the grain growth in the unreacted film contributes to the resistivity *decrease* [Murarka 1983].

For sample Y and Z the amorphous silicon oxide layer acted as a protection against plasma damage, which does not contribute to increase the resistivity. However, the oxide layer slows down the diffusion of the Pt atoms into silicon. In the early steps of silicide formation an amorphous Pt + Si layer is often seen at the silicide/silicon interface [Abelson 1988]. For samples with an interfacial oxide layer, the amorphous Pt + Si layer is seen up to 250 °C. This contributes to an *increase* of the sample resistivity. We suppose that the constant resistivity value is obtained by a mutual compensation between the two previously mentioned processes: crystalline order increases in the Pt unreacted film (resistivity decreases) whereas Pt atoms diffuse to form an amorphous silicide layer (resistivity increases).

At 600 °C, PtSi facets appear, due to Si recrystallization at the silicide/silicon interface. Recrystallization progresses from the silicide/Si interface towards the Si surface, along the grain boundaries. As explained in Chapter IV, the 'newly-created' PtSi facet separates progressively each grain from its neighbor. Grains are connected only by their upper part. The film conductivity is essentially determined by the decreasing thickness of the upper, continuous region. At 650 °C these facets

thicknesses are the sum of silicide and unreacted Pt thicknesses. For sample X, without the interfacial oxide layer, the unreacted Pt seen in the as-deposited film, above the silicide/Pt interface, disappears at 250 °C. For samples Y and Z, with an interfacial oxide layer, the unreacted Pt film is seen at least up to 550 °C. At 600 °C it disappears for sample Y and becomes discontinuous for sample Z.

Resistivity values obtained for the three samples (~ 30 μΩcm) are in good agreement with data from Murarka [Murarka 1983] and Sinha [Sinha 1972]. The three samples show a similar qualitative resistivity behavior as a function of the annealing temperature: the presence of the interfacial oxide layer, even as thick as 2.2 nm, does not change substantially the transport properties as a function of the annealing temperature. *The lowest resistivity value (~ 30 μΩcm) does not depend on the presence or the thickness of the oxide interfacial layer. It is the same for the three samples.*

Small differences can be seen between as-deposited samples (165 °C) and 250 °C-annealed samples: samples X show the expected decrease in the resistivity whereas samples Y and Z show a constant value. However, for the three samples, resistivity values converge to a common value at 250 °C and at 350 °C.

Sample X keeps its resistivity unchanged up to 600 °C. Samples Y and Z still show a slight decrease up to 500 °C, followed by a slight increase between 500 and 550 °C. Once again the resistivity values converge at 550 °C for the three samples. In terms of transport quality, *it is very important to point out that, as soon as the increasing in resistivity is detected in a sample, measurements fluctuates and the electrical conduction is less stable than before. This indicates that an irreversible transformation is occurring which leads to film degradation.*

Above 600 °C, we see a resistivity increase for all samples, but it is faster for samples X and Z than for sample Y. We measured the substrate resistivity above 700 °C for sample X and Z and above 750 °C for sample Y. As we will see in the

become more pronounced; some large grains become even deeper by incorporating their neighbors. In this process, the smaller grains whose atoms migrate to the larger grains become thinner and then disappear. The *effective conduction thickness* is, therefore, given by the thickness of the thinnest grain. For sample Z it is, at 600 °C, 3.1 nm (Fig. V.3).

At 700 °C, samples X and Z are discontinuous. Sample Y is not discontinuous yet, due to an 8 nm-deep contact region between PtSi grains through the boundaries, and a continuous Pt_2Si sub-layer (~ 10 nm-thick), still present at the top of the silicide layer. Above 700 °C, as foreseen by the phase diagram, Pt_2Si disappears. Sample Y shows a resistivity $\rho < (4 \times 10^{-4}\ \Omega cm)$ at 750 °C. Above 750 °C all samples are discontinuous.

The reason why the film becomes discontinuous, and consequently, the resistivity increase occurs at different temperatures for the three samples is discussed below:

- In sample X, without interfacial oxide, all of the available Pt has reacted, and all of the PtSi has already formed at 350 °C. As the Si recrystallization starts, the PtSi layer forms islands.

- In samples Y and Z, with interfacial oxide, unreacted Pt can be found up to 700 °C. Island formation depends on the interfacial oxide thickness in the following way:

a) In sample Z, with 2.2 nm-thick interfacial oxide, two mechanisms are in competition: on the one hand there is Pt_2Si formation that increases the silicide film thickness; on the other hand, the re-ordering of the PtSi already arranged in islands. Since the oxide is thick, the Pt diffusion is limited (the remaining unreacted Pt is non-negligible and the silicide film is thinner in this sample) and the PtSi re-ordering becomes faster. This is clearly observed even at 600 °C. Thus, the PtSi re-ordering predominates and the film becomes discontinuous above 650 °C.

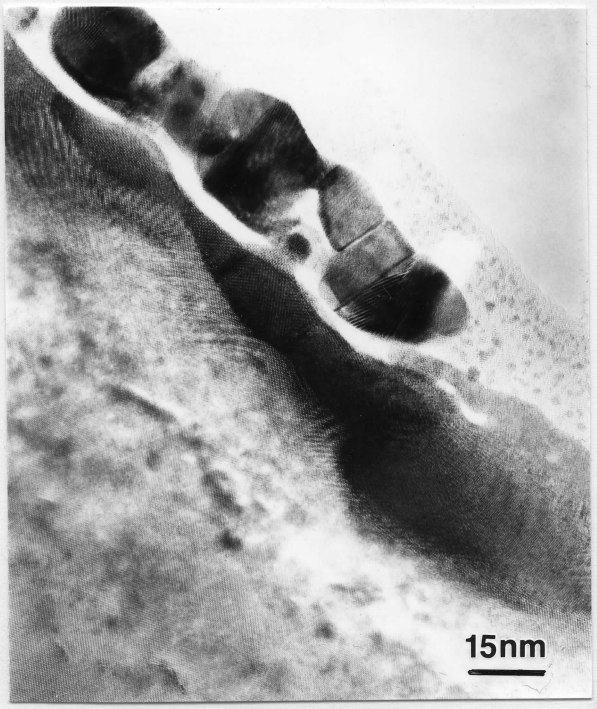


Fig. V.3: TEM image of sample Z annealed at 600°C.

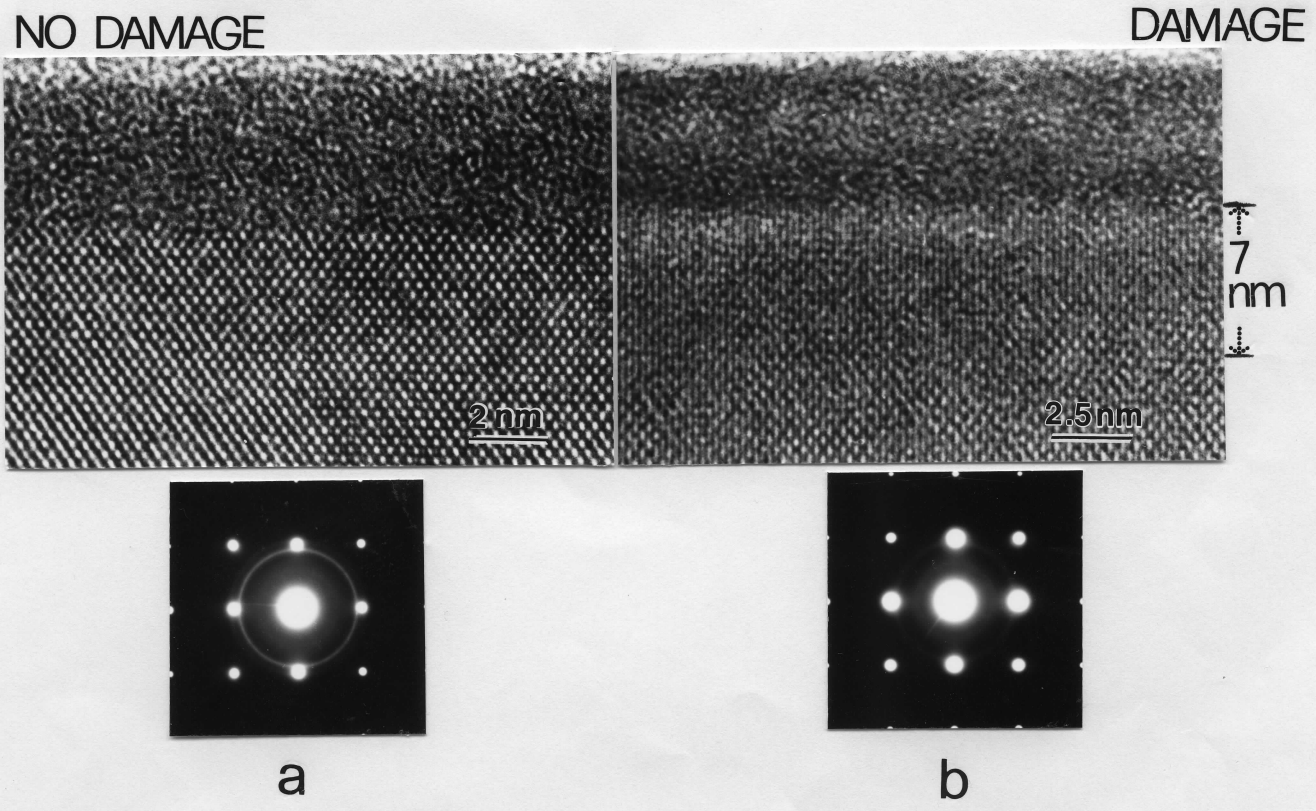


Fig. V.4: HRTEM cross-sectional images (taken in Si[110] direction) and ED pattern (taken in the Si[001] direction) of the as-deposited samples: a) A; b) D.

b) In sample Y, with a thin oxide layer, unreacted Pt diffuses under the controll of the oxide barrier. The reaction speeds (Pt_2Si formation, PtSi formation and re-ordering) remain in equilibrium until the complete consumption of all the available unreacted Pt, between 650 and 700 °C. The Pt_2Si layer that was continuous and homogeneous in thickness up to 700 °C disappears above this temperature. The remaining contact between PtSi grains becomes smaller and smaller, until discontinuity sets in above 750 °C. The controlled Pt diffusion by the 1.3 nm-thick interfacial oxide layer is actually beneficial, slowing down the resistivity increase caused by island formation.

Sinha et al. [Sinha 1972] found an approximately similar qualitative resistivity behavior as a function of annealing temperature for 20 nm-thick PtSi films on Si(111). These authors report a progressive decrease in resistivity up to 850 °C, due to grain growth and a decrease in grain boundary contribution to resistivity. They found an abrupt increase at 900 °C due to agglomeration at this temperature. They also observe a less drastic resistivity increase for 90 nm-thick films at the same temperature. There are similarities and discrepancies between Sinha's studies and ours. Although Sinha's samples have a crystallographic orientation different from ours, we see the same resistivity evolution as a function of the annealing temperature, in intimate relationship with the morphological silicide film changes. The discrepancies are correlated to the temperature at which morphological transformations occur and the role played by the grain size increase. Concerning the differences in morphological transformation temperature they seem to be related to crystallographic changes that are not the same if we use a Si[111] or a Si[100] substrate. Concerning the role of the grain size increase, Sinha did not give us information about the homogeneity of the grain size during the grain growth process. However, for silicide films on Si[100] substrates, the increasing inhomogeneity in grain size and depth is the main factor to quickly increase the resistivity.

From the results of this section we observe that the presence of interfacial oxide has little effect on the final film resistivity. However, it is worth noting that certain have the same resistivity while displaying different morphologies: only *insignificant*

differences are seen in the resistivity behavior as a function of the annealing temperature in silicide films on Si[100] with and without interfacial silicon oxide layer in the 250 - 550 °C range. For all the three types of films, the resistivity is approximately the same (~ 3 x 10^{-5} Ωcm) over this temperature range and all of them are equally useful in practical applications. The maximum annealing temperature compatible with low resistivity depends on the possibility of slowing down island growth, which leads to film discontinuity. The thin interfacial oxide barrier can do this, but it is not easy to control the chemical etching to obtain the right oxide thickness. However, it is possible to obtain the same effect using other preparation methods as discussed in the following section.

V.3 Ultrathin silicide films on substrates with plasma etching damage

Plasma etching appears to be a simple and clean process to eliminate residual superficial native silicon oxide prior to Pt deposition. The drawback is that structural damage is inflicted to the substrate. We will show that by an appropriate dosage of the beam exposure, the substrate damage can be almost completely annealed before island formation starts taking place in the silicide layer.

V.3.1 4.0 - 4.6 nm-thick platinum silicide films

The resistivity can be increased by plasma damage depth on the substrate surface with respect to a non-bombarded sample. However, a certain dose of plasma damage can be beneficial in slowing down the Si recrystallization that leads to an epitaxial and island-type PtSi film. As soon as all substrate damage has been annealed, silicide island formation and epitaxy set in.

In this section we study the resistivity as a function of the annealing temperature for four platinum silicide films prepared on Si substrates with different depth of plasma etching damage. One of the samples was not plasma-bombarded, to be compared with the others. In Fig. V.4 we can see the cross-sectional HRTEM image of two of the four as-deposited samples analyzed in this section (samples A and D) and the corresponding Electron Diffraction (ED) patterns. The Pt metal layer always completely covers the Si surface. No interfacial oxide is detected between the metallic film and the Si substrate surface in all cases. We observe that metallic film thicknesses fall in a very narrow range whereas Si substrates show a very different plasma damage depth. The ED for these samples show broad rings (superimposed on the spots coming from the monocrystalline Si substrate, in [100] direction), indicating that the metallic films are mostly amorphous. We found broad rings present at Pt positions (for the four samples) and, also at PtSi and Pt_2Si positions for two of the four samples, but they are weak and not well defined.

Measurements of the metallic film thickness and plasma etching damage on the substrate were taken from micrographs similar to that of Fig. V.4 for the four samples mentioned above:

Sample A: (4.4 ± 0.3) nm - thick metallic film; 0 nm damage depth

Sample B: (4.6 ± 0.3) nm - thick metallic film; (2.5 ± 0.4) nm damage depth

Sample C: (4.0 ± 0.3) nm - thick metallic film; (4.5 ± 1.1) nm damage depth

Sample D: (4.5 ± 0.2) nm - thick metallic film; (7.2 ± 1.5) nm damage depth

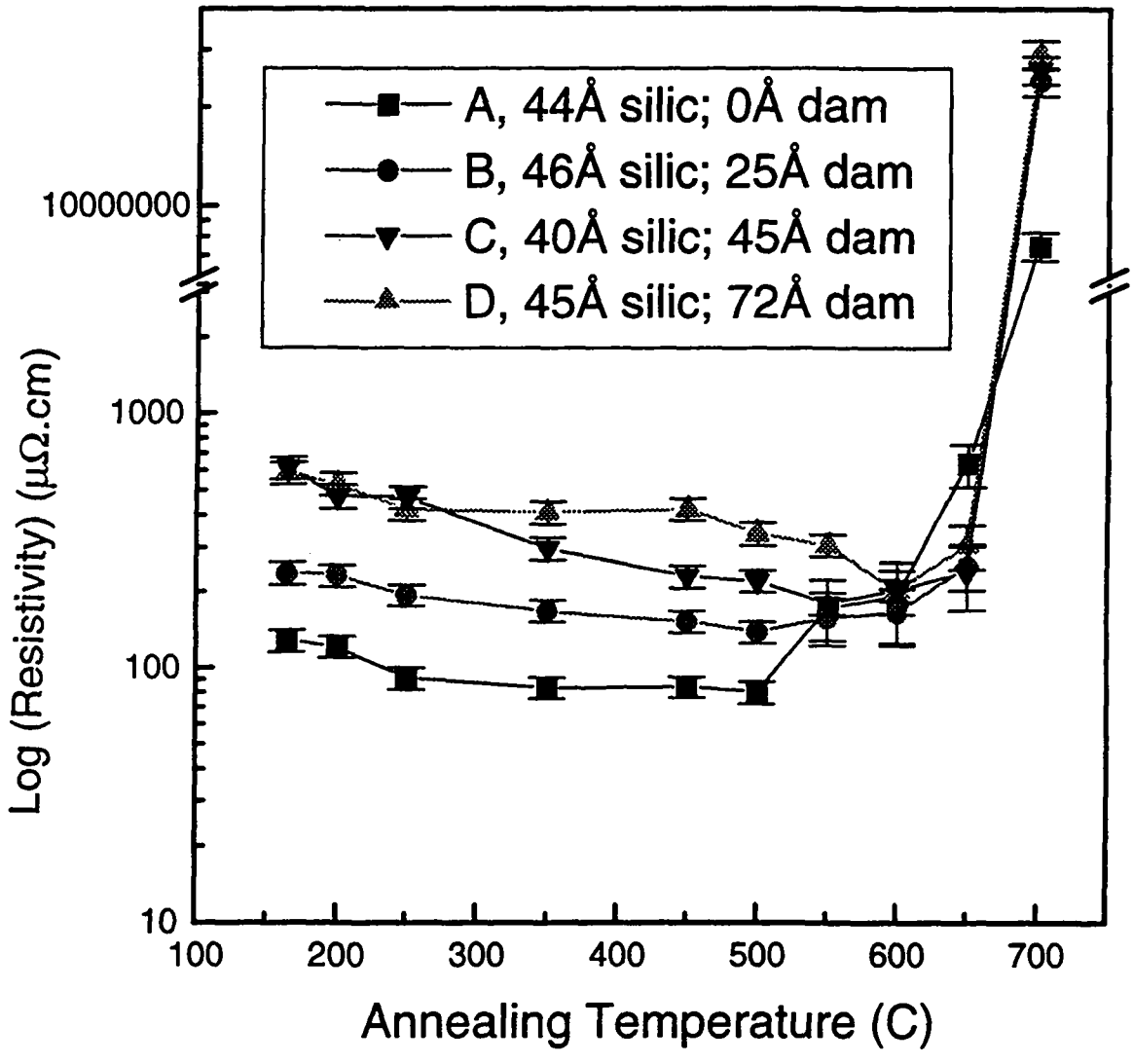


Fig. V.5 - Resistivity (in logarithmic scale) as a function of the annealing temperature for 4 - 5 nm-thick silicide films: Sample A: (4.4 ± 0.3) nm-thick metallic film, 0 nm-deep damage; Sample B: (4.6 ± 0.3) nm-thick metallic film, (2.5 ± 0.4) nm-deep damage; Sample C: (4.0 ± 0.3) nm-thick metallic film, (4.5 ± 1.1) nm-deep damage; Sample D: (4.5 ± 0.2) nm-thick metallic film, (7.2 ± 1.5) nm-deep damage.

In Fig. V.5 we show the resistivity as a function of the annealing temperature for samples A, B, C and D. The lowest resistivity line corresponds to sample A (without substrate damage) and the highest resistivity line to the sample D (deepest substrate damage). The two intermediate lines correspond to the two intermediate substrate damage depths, in increasing order. The silicide film thickness being quite similar, the differences in the silicide resistivity baseline value are determined by the substrate damage depth near the silicide/silicon interface.

165 °C-annealed samples show a high resistivity. As the annealing temperature increases, resistivity values decrease, as expected. This can be observed even for 200 °C-annealed samples. This tendency is observed up to 500 - 600 °C temperature range. Percentual decreasing values for each sample and the temperature range in which it occurs are listed below:

Sample	Percentual resistivity decrease (%)	Temperature range (°C)
A	60	165 - 500
B	70	165 - 500
C	239	165 - 550
D	188	165 - 600

Table V.1 - Percentual resistivity decrease in the various annealing temperature range.

In this table we see that small percentuals of decreasing resistivity correspond to the small temperature range (165 - 500 °C) in which resistivity decreases. On the other hand, larger percentuals of decreasing resistivity correspond to larger temperature

range (165 - 600 °C) in which resistivity decreases. The amount of resistivity decrease is correlated to the different resistivity behavior between 500 and 600 °C (see Fig. V.5), which we discuss below:

- between 500 and 550 °C, samples with the deepest damage (C and D) still show a decreasing resistivity, whereas samples without substrate damage and shallow substrate damage (A and B) show a reversal in the resistivity trend. For sample A the resistivity increases by 115% for sample A and by 20% for sample B in the mentioned range of temperature. *As we said previously, the resistivity increase leads to a discontinuous, electrically useless film.*

- between 550 and 600 °C the only sample that still presents a decreasing resistivity is the sample with the deepest substrate damage (sample D).

- at 600 °C, the resistivity of all samples converges towards a common value (~ 2 x 10^{-4} Ωcm). The resistivity increases after annealing above 600 °C. At 650 °C it reaches a common value (~ 3 x 10^{-4} Ωcm) for samples B, C and D and a higher value for sample A (7 X 10^{-4} Ωcm). Above 650 °C, measurements give us the Si substrate resistivity for all samples, indicating that the films are fully discontinuous.

The resistivity evolution as a function of the annealing temperature can be explained by the structural and morphological transformations observed in these films. From both analyses we can establish an important correlation: films that have low and/or decreasing resistivity show an homogeneous morphology with a narrow grain size distribution. When larger grains start to form the resistivity increases. This behavior becomes more pronounced when we the local discontinuity appears in the film due to the consumption of the small grains.

Fig. V.6 shows SEM micrographs of sample B ((4.6 ± 0.3) nm - thick metallic film; (2.5 ± 0.4) nm damage depth) where the film morphology at different annealing

temperatures is analyzed. SEM images confirm that as-deposited films show no grain structure (grains are probably smaller than the SEM resolution) and that they can be considered amorphous, as showed by the HRTEM images and ED patterns in Fig. V.4. The subsequent decrease in resistivity can be attributed to an increase of the crystallographic order in the silicide layers. In pictures of 500 °C-annealed samples, there is an homogeneous grain structure (Fig. V.6a) corresponding to the lowest resistivity value ($(1.4 \pm 0.1) \times 10^{-4}$ Ωcm). Between 500 and 550 °C the slight increase in resistivity is accompanied by the growth of large grains that coexist with small grains.

In the 550 °C-annealed sample micrograph (Fig. V.6b) we see the small grains between larger, ligther grains, that are surrounded by dark areas. These are regions where the substrate surface is no more covered by the silicide film. This is a consequence of the grain size increasing by incorporations of the surrounding small grains. This behavior is confirmed in 600 °C-annealed samples (Fig. V.6c), where the number of large grains and the surrounding exposed Si surface are high. The image of the 650 °C-annealed sample (Fig. V.6d) shows the discontinuous character of the silicide film, formed by large and isolated islands.

In SEM images (Fig. V.7i) we can also compare the morphology of the four silicide films at 550 °C. The three samples with shallower damage and similar resistivity values at 550 °C do not show an identical film morphology: samples A and B, which reach a resistivity of (2×10^{-4} Ωcm) by *increasing* the resistivity show large and small grains (the same kind of contrast as in Fig. V.6), meanwhile samples C and D, that reach the same resistivity value (2×10^{-4} Ωcm) by *decreasing* the resistivity, show a quite homogeneous grain size. We observe that increasing resistivity is related to island formation and decreasing resistivity, to continuity and homogeneity in grain size, even if the resistivity value reached is the same. This tendency is even more pronounced at 600 °C (Fig. V.7ii) for samples A, B and C that show large and

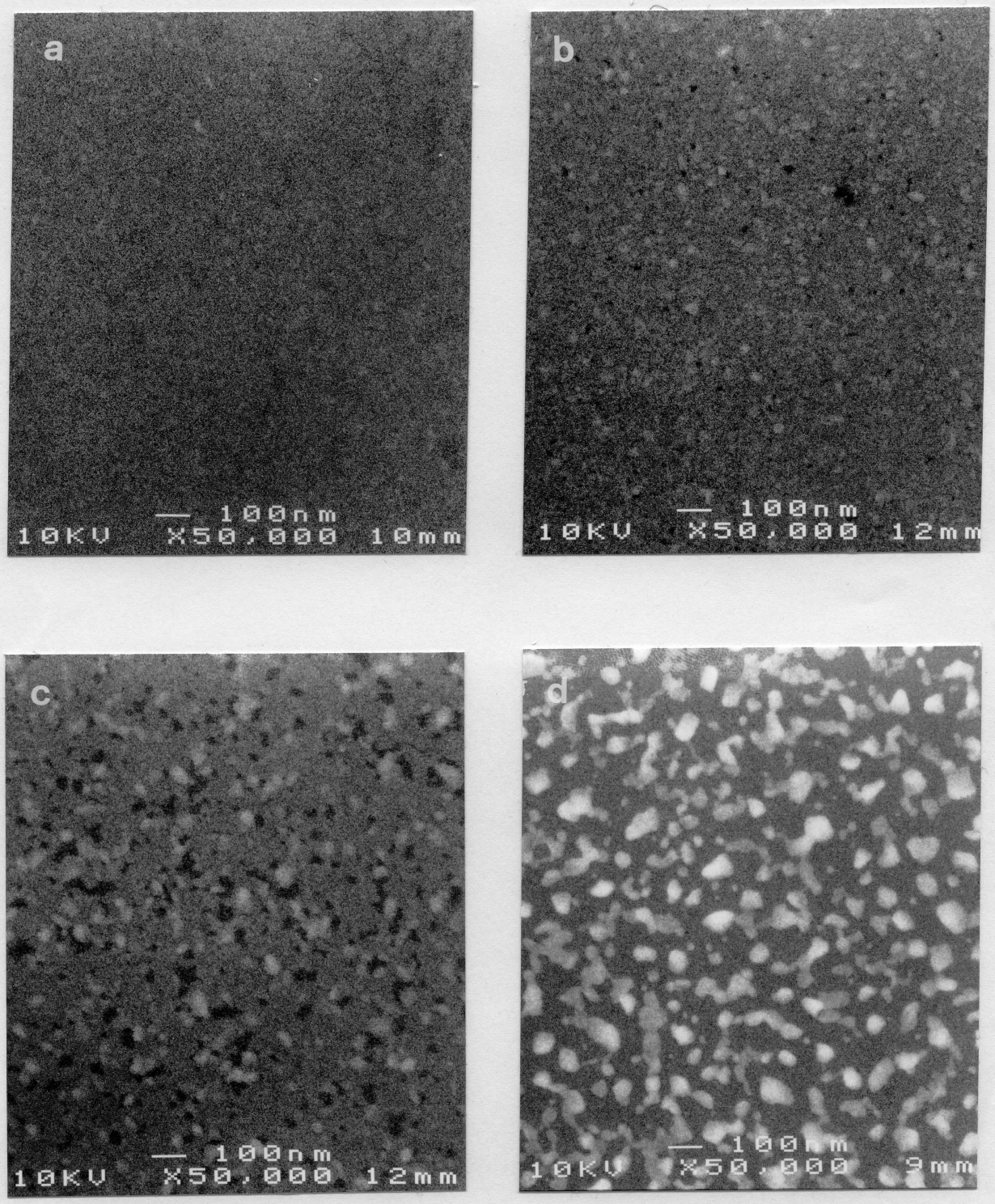


Fig. V.6 : SEM images of sample B (46 Å-thick silicide; 25 Å-deep damage) annealed at: a) 500 °C ; b) 550 °C c) 600 °C d) 650 °C. The Si substrate is seen as dark regions, while small and large PtSi grains are ligther.

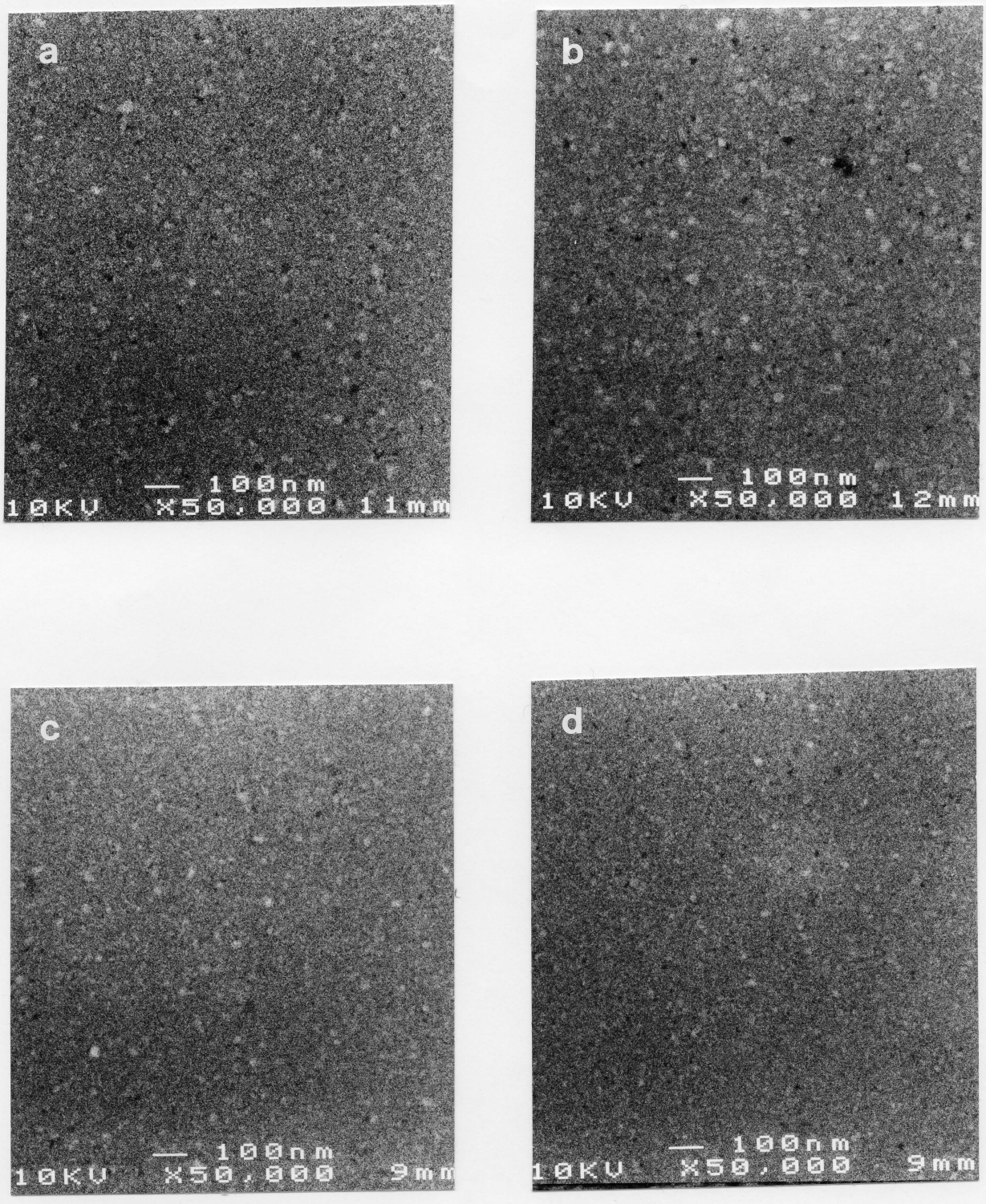


Fig. V.7i : SEM images of samples: a) A ; b) B ; c) C ; d) D , annealed at 550 °C. We can observe the growing of large PtSi grains inducing some film discontinuity (we can see dark regions corresponding to the substrate) mainly in samples A and B.

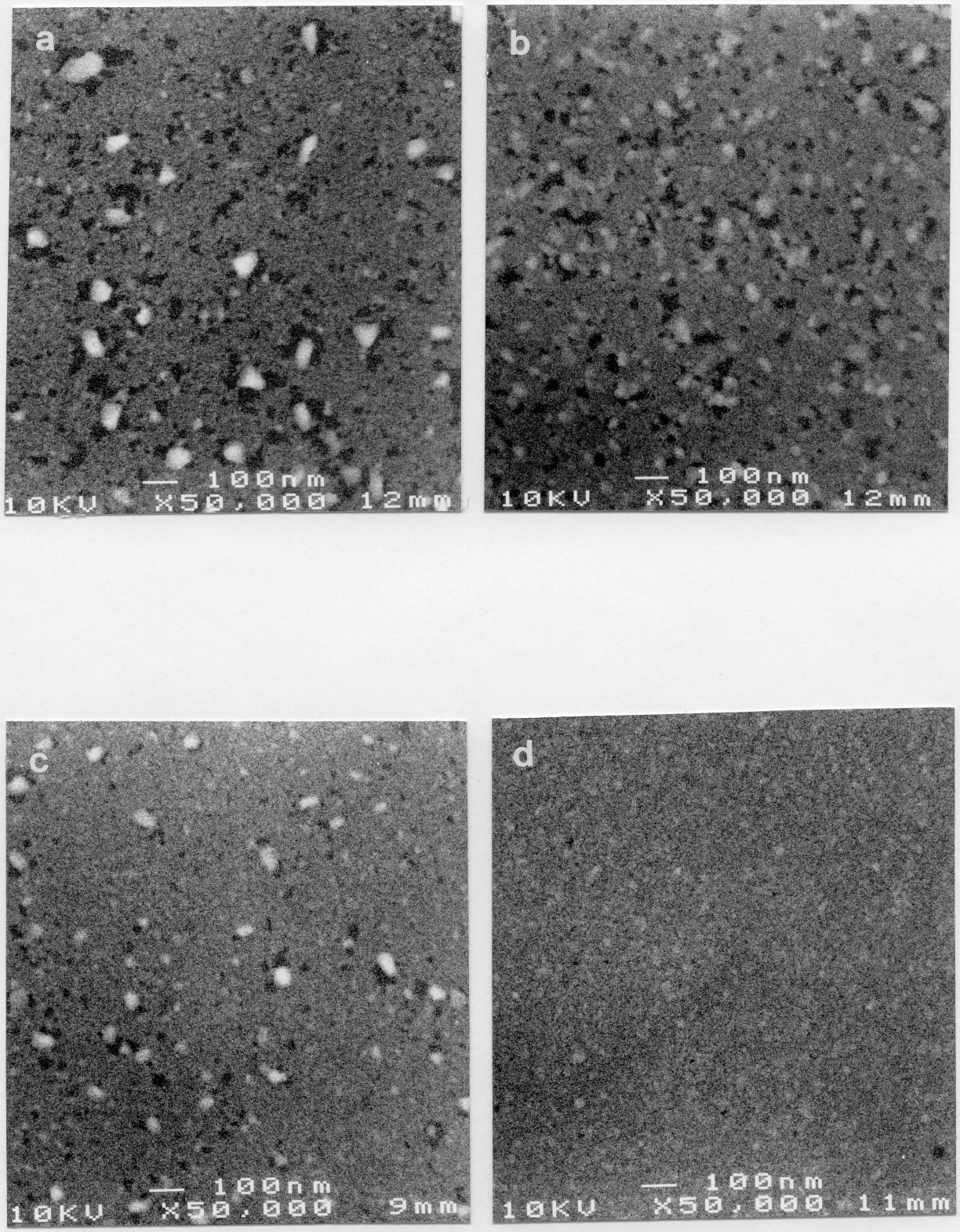


Fig. V.7ii : SEM images of samples: a) A ; b) B ; c) C ; d) D , annealed at 600 °C. The contrast in micrographs of samples A, B and C shows an inhomogeneity in grain size (small and large PtSi grains, light regions) and a clear tendency to discontinuity, exhibiting the surface substrate (dark regions, surrounding large grains)

partially isolated grains, whereas sample D, the only one that still shows decreasing resistivity, shows a few large grains but the majority of grains are still small. We observe film discontinuity around the large grains (they incorporated small grains of their vicinity) but it is still infrequent at 600 °C. However, all samples become discontinuous infrequent at 600 °C. However, all samples become discontinuous between 650 and 700 °C.

There is a direct correlation between the plasma etching damage depth and the temperature at which morphological transformation occurs. The samples without plasma etching damage change their morphology at the lowest temperature, whereas the samples with the deepest plasma etching damage are the samples that maintain continuity for the longest time and change their morphology at the highest temperature. Thus, *the residual plasma etching damage plays an important role in slowing down the agglomeration.* In the next section we will discuss this point further.

V.3.2 2.9 - 3.5 nm-thick platinum silicide films

The ultra-thin nanometric films are the most delicate to process successfully. 3 nm-thick thin films are even more sensitive to process conditions that 5 nm-thick films. We analyzed the resistivity as a function of the annealing temperature for films as thin as 2.9 nm, with different plasma etching damage depth on substrate surface. We observed that the electrical performance and the slowing down of the island formation can be improved by creating a shallow damage on the substrate, using an appropriate dose of plasma etching. Photovoltaic applications can, effectively, benefit from such film structures.

Figure V.8 shows the cross-sectional HRTEM images for two of the five as-deposited samples analyzed in this section (sample M and Q). Except for the metallic film thickness, these samples are similar to samples A - D. Silicide film thicknesses and

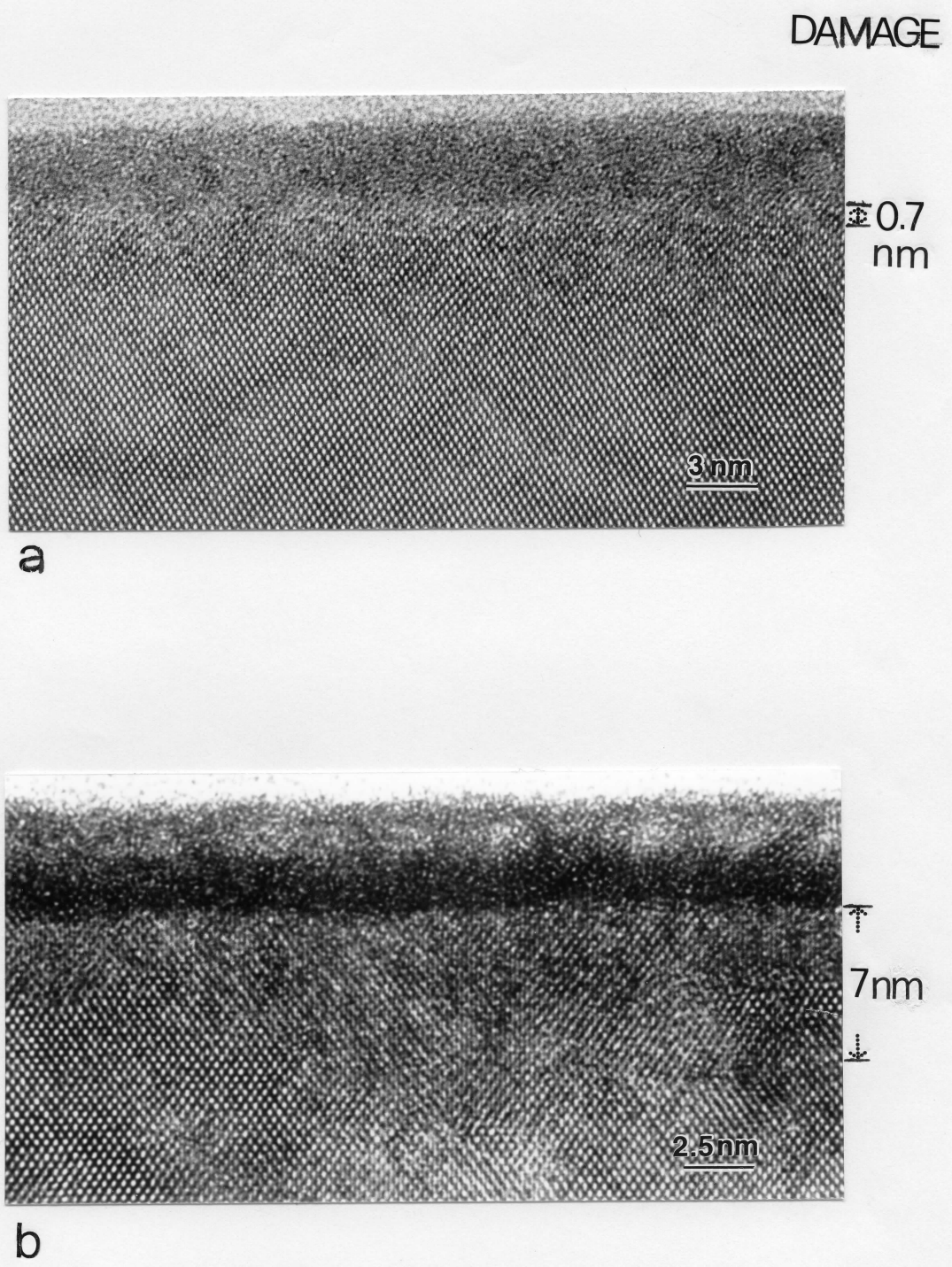


Fig. V.8: HRTEM cross-sectional images of the following as-deposited (165 °C-annealed) samples: a) M; b) Q.

plasma etching damage depth on substrate surface were obtained from this kind of micrographs:

Sample M: (3.0 ± 0.4) nm-thick platinum silicide film; (0.7 ± 0.2) nm-deep damage

Sample N: (3.1 ± 0.3) nm-thick platinum silicide film; (1.5 ± 0.3) nm-deep damage

Sample O: (2.9 ± 0.3) nm-thick platinum silicide film; (1.9 ± 1.0) nm-deep damage

Sample P: (3.3 ± 0.5) nm-thick platinum silicide film; (3.1 ± 1.4) nm-deep damage

Sample Q: (3.5 ± 0.3) nm- thick platinum silicide film; (7.5 ± 1.6) nm-deep damage

We analyzed the evolution of the resistivity of these samples as a function of the annealing temperature. The values obtained are shown in Fig.V.9.

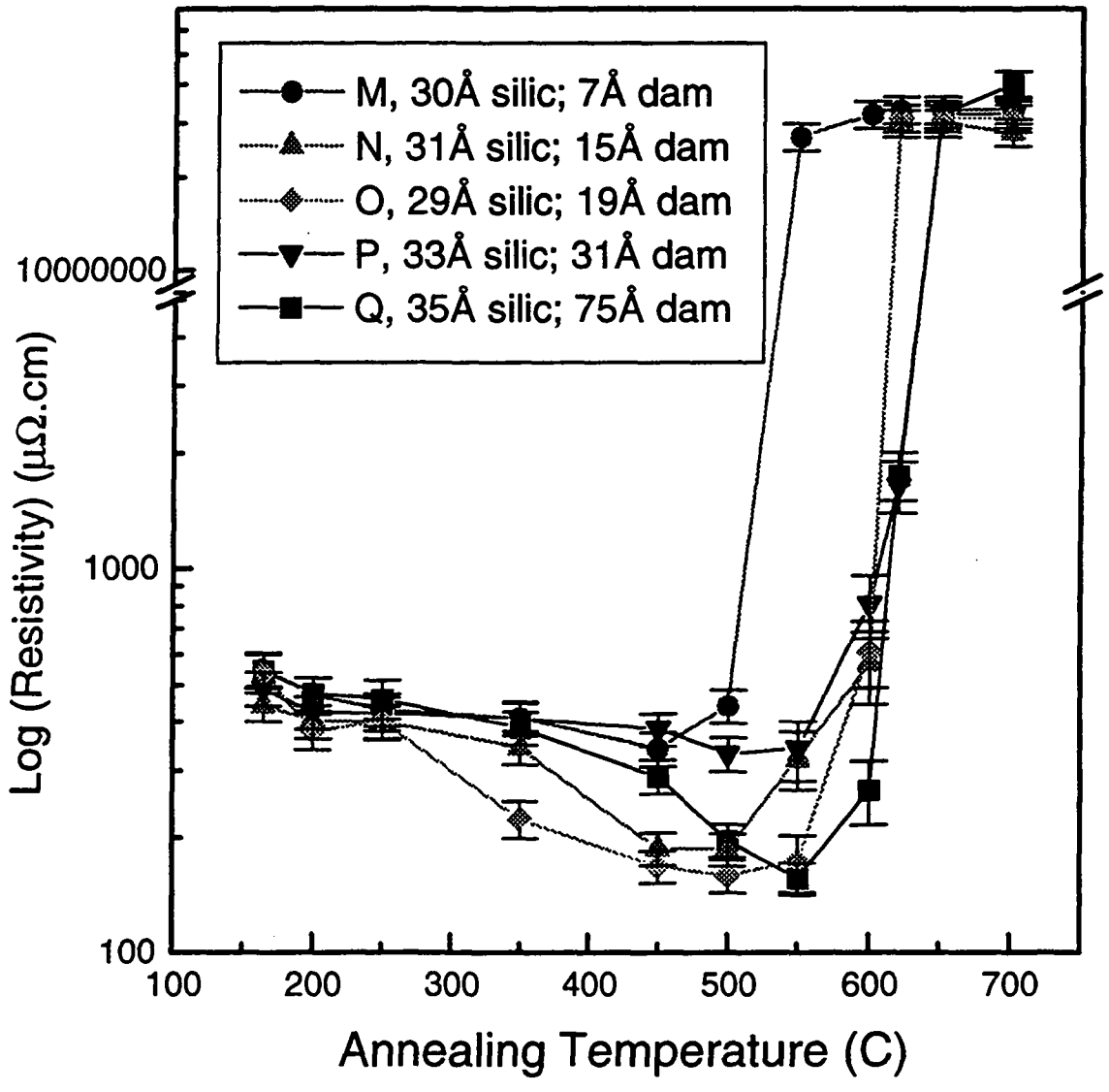


Fig. V.9 - Resistivity (on a logarithmic scale) as a function of the annealing temperature for very thin silicide films. Sample M: (3.0 ± 0.4) nm-thick metallic film, (0.7 ± 0.2) nm-deep damage; sample N: (3.1 ± 0.3) nm-thick metallic film, (1.5 ± 0.3) nm-deep damage; sample O: (2.9 ± 0.3) nm-thick metallic film, (1.9 ± 1.0) nm-deep damage; sample P: (3.3 ± 0.5) nm-thick metallic film, (3.1 ± 1.4) nm-deep damage; and sample Q: (3.5 ± 0.3) nm-thick metallic film, (7.5 ± 1.6) nm-deep damage.

Once again the resistivity decreases with increasing the annealing temperature. However, all five samples show quite similar resistivity values when annealed between 165 and 250 °C. Above 350 °C we have a spread in the resistivity evolution: sample M (with the shallowest damage), P and Q (with the deepest damage) maintain a high resistivity, whereas samples N and O show an important decrease in resistivity up to 450 °C.

Above 450 °C the resistivity evolution of the five sample is different. Sample M shows increasing resistivity above 450 °C reaching the Si substrate resistivity (evidence of silicide film discontinuity) above 500 °C. This sample shows the highest resistivity values after annealing at intermediate temperatures (450 - 550 °C), i.e. ((3.5 ± 0.5) x 10^{-4} Ωcm). Sample N keeps its resistivity unchanged between 450 and 500 °C and sample O, P and Q show a resistivity decrease in the same temperature range. Between 500 and 550 °C, samples N, O and P show a slight resistivity increase but not sample Q, which still shows a decreasing resistivity. In particular, sample Q reaches the lowest resistivity value of this measurement set ((1.5 ± 0.1) x 10^{-4} Ωcm) at 550 °C. At 600 °C samples N, O and P reach (0.6 - 1) mΩcm, while sample Q just slightly increases its resistivity to (100 - 200) μΩcm range. Above 600 °C, samples N and O show the substrate resistivity. Samples P and Q reach (1.0 - 1.1) mΩcm at 620 °C (slow resistivity increase for sample P and fast increase for sample Q) and become discontinuous above this temperature.

The differences in resistivity evolution as a function of the annealing temperature are related to the morphological and structural evolution and shown by SEM, HRTEM and ED analyses.

V.3.2.1 SEM analyses

Films annealed between 165 and 250 °C show no grain structure by SEM, which means that they are mostly amorphous or short-range ordered. This information is in good agreement with the relatively high (and similar) resistivity for these five films.

Concerning the 'spread' in the resistivity evolution between 350 °C and 450 °C, different resistivities are also correlated to differences in morphology. Figure V.10 show SEM images for samples M (high resistivity) and samples O (decreased resistivity). Sample M shows large and small grains meanwhile sample O shows only small grains, with a homogeneous grain size distribution.

At 500 °C, however, the difference in resistivity tendency between sample M and the others is justified by differences in film morphology: samples N, O, P and Q are continuous but sample M already shows the tendency to form islands. The growth of large grains, already seen at 450 °C, improves film discontinuity. Samples N and Q, which still have low resistivity, show a more uniform silicide film, with some rare occurrences of large grains. Sample N, in particular, show a textured film. In Fig. V.11 we can see a morphology comparison between samples M, N and Q annealed at 500 °C.

Samples annealed between 500 and 600 °C show two different resistivity evolutions: samples N, O and P keep high resistivity and/or increase resistivity quickly, reaching high intermediate resistivity (0.6 - 1 mΩcm) at 600 °C; sample Q shows low resistivity ($\rho < 2 \times 10^{-4}$ Ωcm) up to 550 °C and a slow resistivity increase between 550 and 600 °C ($\rho < 3 \times 10^{-4}$ Ωcm at 600 °C). The morphology of samples N and Q at 550 and 600 °C are compared in Fig. V.12. Sample N shows a more pronounced tendency to discontinuity than sample Q at 600 °C (Fig. V.12b). In fact, we can see in this micrograph many regions of a *particular kind of film discontinuity* where only a part of small grains were incorporated by large grains, as already seen in the previous section. *The remaining small grains form a network connecting large grains.* The electric current can pass through this network and not through the substrate. This is the morphologic silicide film configuration that gives a resistivity of

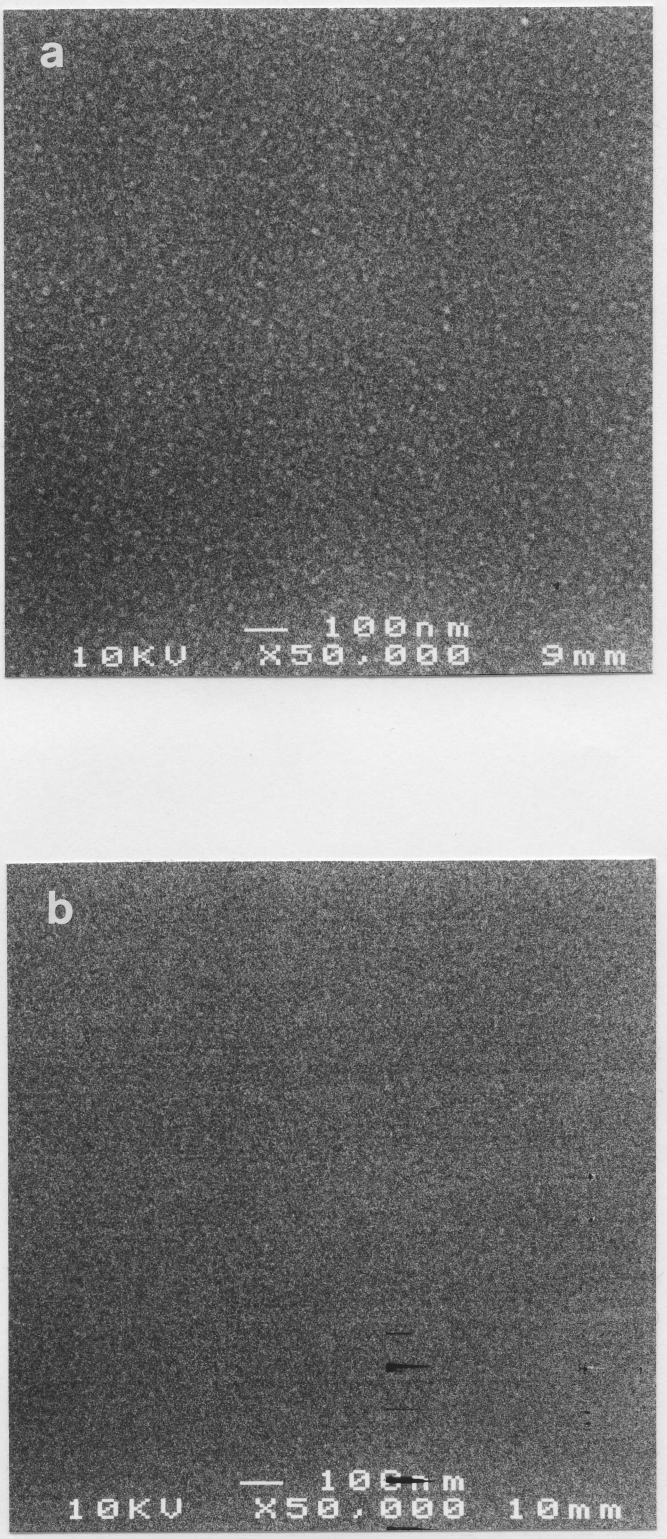


Fig. V.10 : SEM images of samples: a) M (high resistivity) and b) O (low resistivity), annealed at 450 °C. Sample M shows large and small grains meanwhile sample O shows only small grains, with an homogeneous size distribution.

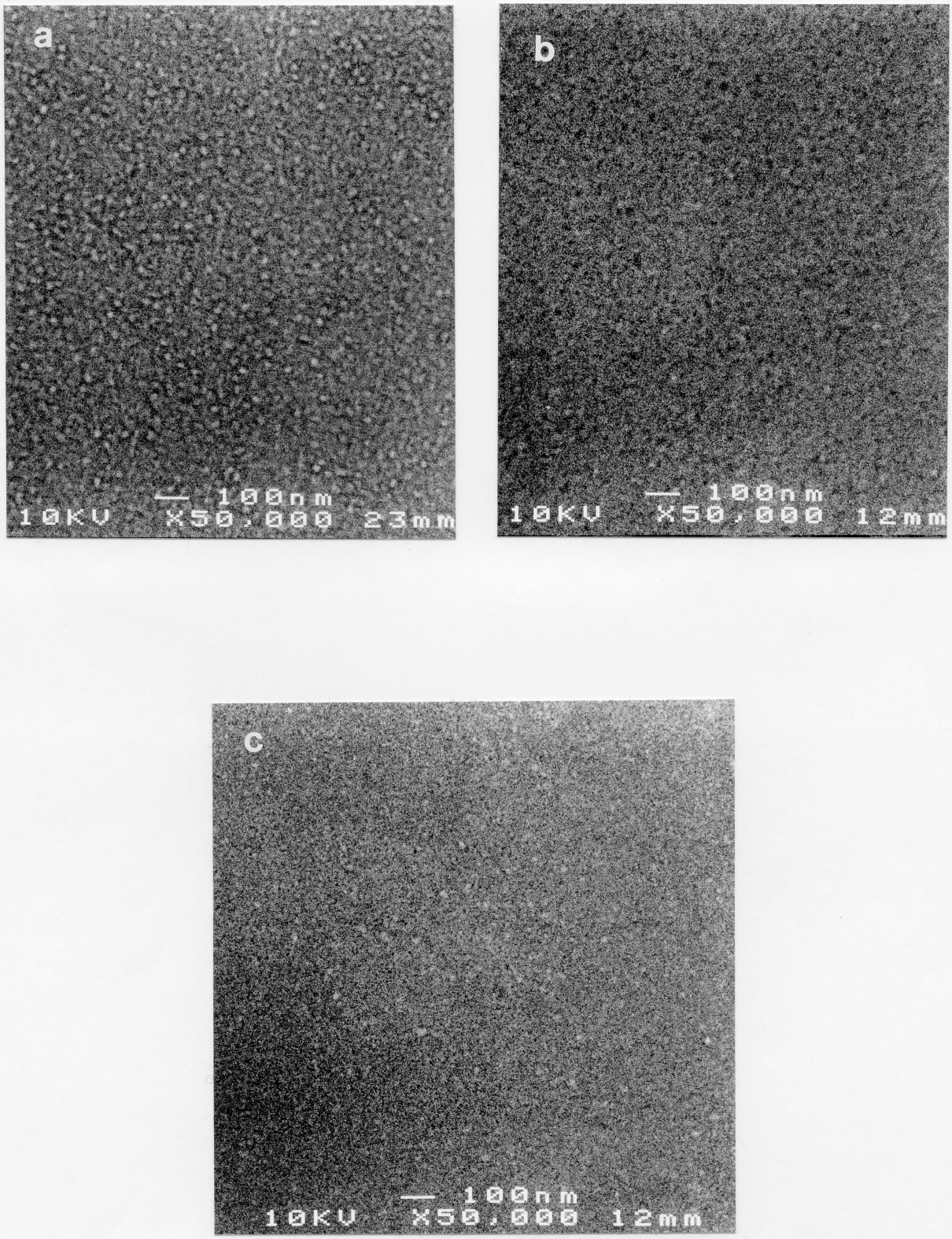


Fig. V.11 : SEM images of samples annealed at 500 °C: a) M ; b) N and c) Q, showing an increasing homogeneity and continuity (from M to Q).

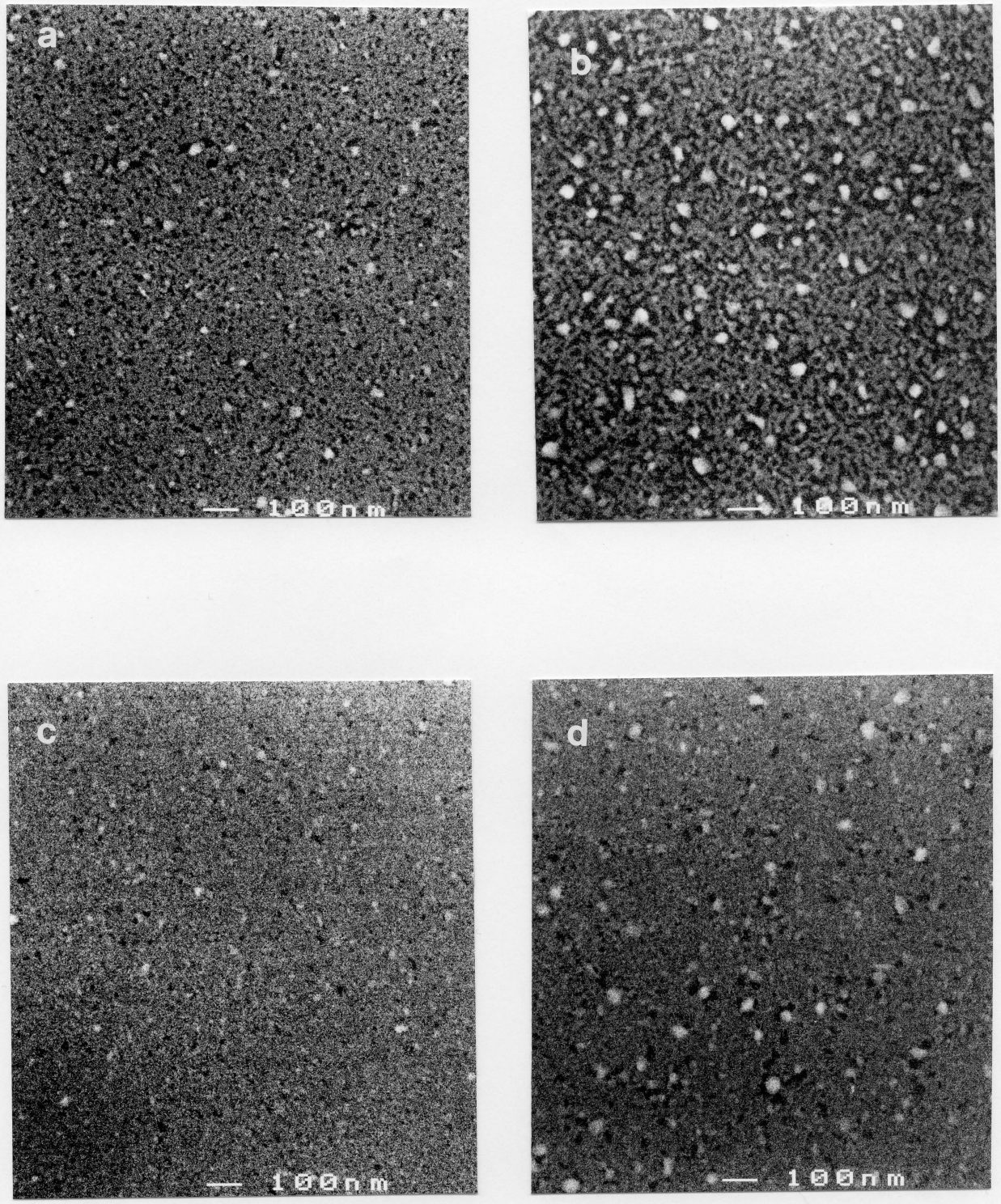
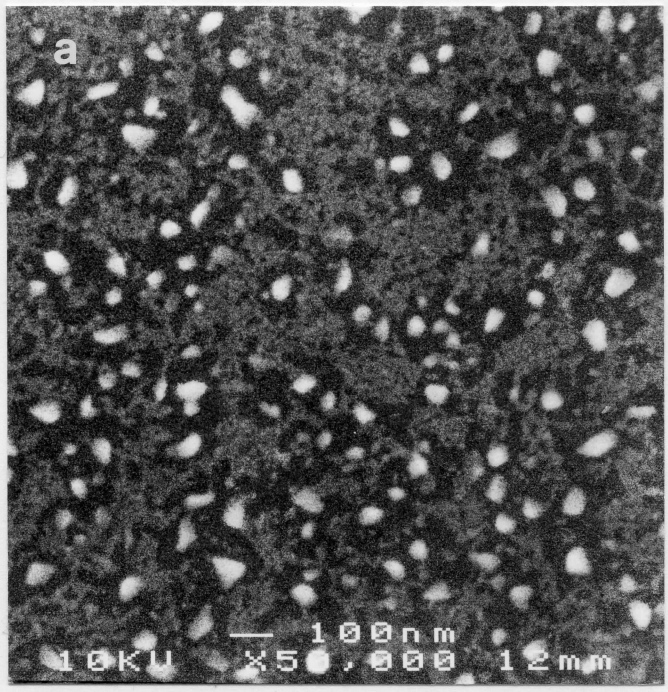


Fig. V.12 : SEM images of **sample N** annealed at : a) 550 °C and b) 600 °C : we can observe that mycelles interconnect large grains. **Sample Q**, annealed at : c) 550 °C ; d) 600 °C.



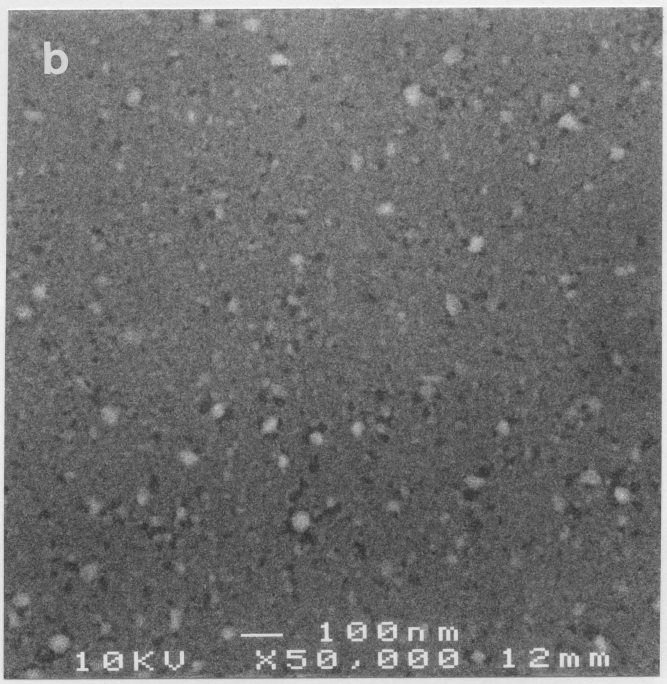


Fig. V.13 : SEM images of samples annealed at 620 °C: a) P, showing mycelles and b) Q, without mycelle formation.

$\rho \sim 1$ mΩcm, an intermediate value between the resistivity of the continuous silicide film and the substrate resistivity. *We called it a 'micelle-like' film.*

At 620 °C, samples P and Q show a resistivity in the ~ 1 mΩcm range. However, they reach the 1 mΩcm resistivity value by slow increasing (sample P) and fast increasing (sample Q). We can observe differences in the morphology related to differences in the resistivity evolution: sample P shows micelles (Fig. V.13a), but sample Q do not (Fig. V.13b). Sample Q showed a continuous film at 600 °C; the discontinuity observed for this sample at 620 °C is not micelle-like type.

V.3.2.3 TEM analyses

The understanding of morphological and structural changes in 2.9 - 3.5 nm-thick silicide films in the 500 - 600 °C annealing temperature range requires further analyses. This information can be obtained from TEM, ED (planar-view preparations) and HRTEM (cross-section preparation) images. The temperature range of interest is 550 - 600 °C, where both morphological and structural changes are observed.

Morphological differences between silicide films annealed at the same temperatures (550 and 600 °C), were observed for the four wafers (N, O, P and Q) by planar-view TEM and ED, as shown in Fig. V.14. The first column of Fig. V.14 shows the micrographs of the 550 °C-annealed samples, which are formed by large and small grains. The corresponding diffraction patterns show that these grains are mostly polycrystalline PtSi as indicated by the presence of rings. Some amorphous silicide is present, as indicated by the broad central ring. But there are also spots in the ED patterns, taken through the Si[100] direction, indicating an epitaxial growth of some silicide planes with respect to the Si substrate.

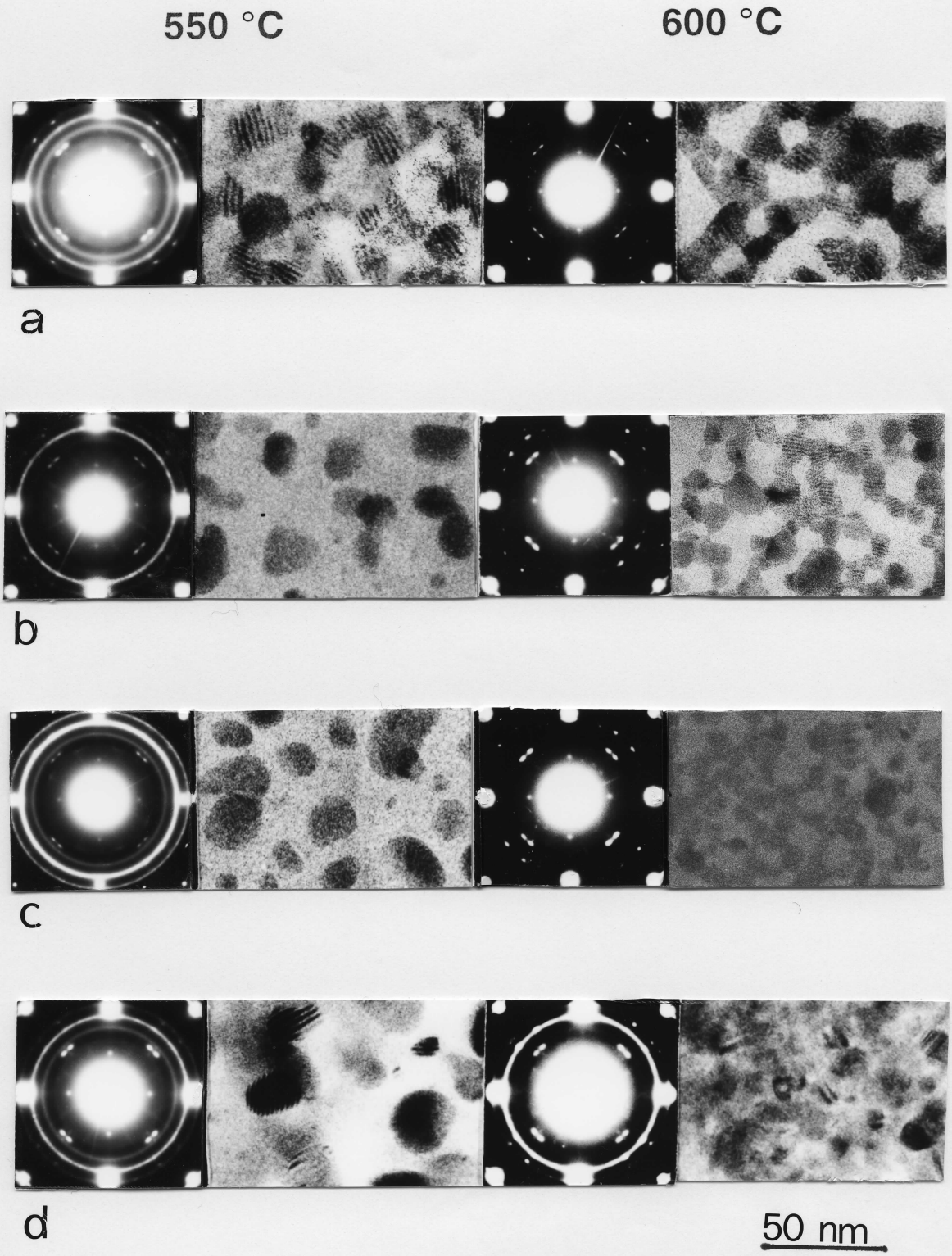


Fig. V.14: Planar-view images and ED patterns of 550 °C- and 600 °C-annealed sample: a) N; b) O; c) P; d) Q. The scale at the bottom of the figure indicates the magnification for all planar-view images.

Some similarities found in the ED patterns for these four samples at 550 °C, indicating a common crystallographic configuration, have been pointed out. The same spots (atomic planes in epitaxial relation with the substrate) and rings (set of atomic planes randomly positioned with respect to the substrate) directions are observed. (A complete crystallographic indexation of these ED patterns can be found in Appendix 2).

The second column in Fig. V.14 shows planar-view images of 600 °C-annealed samples. Figures V.14a, 14b and 14c were taken from samples N, O and P, that show high resistivity at this temperature. As we saw in SEM micrograph of sample N, these silicide films are partially continuous, i.e., constituted by large grains connected by small grains forming a network. TEM analysis shows small grains, aligned, connecting large grains and forming a sort of micelles (micelle = a fiber ordered region) between them. These micelles, observed for the three samples, are more separated in sample N than in sample P. ED patterns show only spots for the three samples, which indicates that these structures are formed exclusively by epitaxial PtSi grains. As we have been demonstrated in Appendix 2 micelle-like films, annealed at 600 °C, are formed by PtSi [1,-1,0] and [1,-2,1] oriented grains, without predominance of one structure with respect to the other.

Figure V.14d shows the planar-view image of sample Q annealed at 600 °C. The film is continuous, formed by an arrangement of large and small grains, as in the 550 °C-annealed sample. ED pattern show the same rings and spots observed for the 550 °C-annealed film. This is an evidence that the structure of the film (polycrystalline + epitaxial grains, with also some amorphous Pt + Si) does not change between 550 and 600 °C annealing temperature. Thus *sample Q, which is continuous and shows low resistivity at 600 °C, keeps a certain amount of polycrystalline grains and even of amorphous Pt + Si at this temperature.*

From Fig. V.13 and 14 we observe that the differences in resistivity for samples annealed at 600 °C are due to morphological and structural reasons. In the next

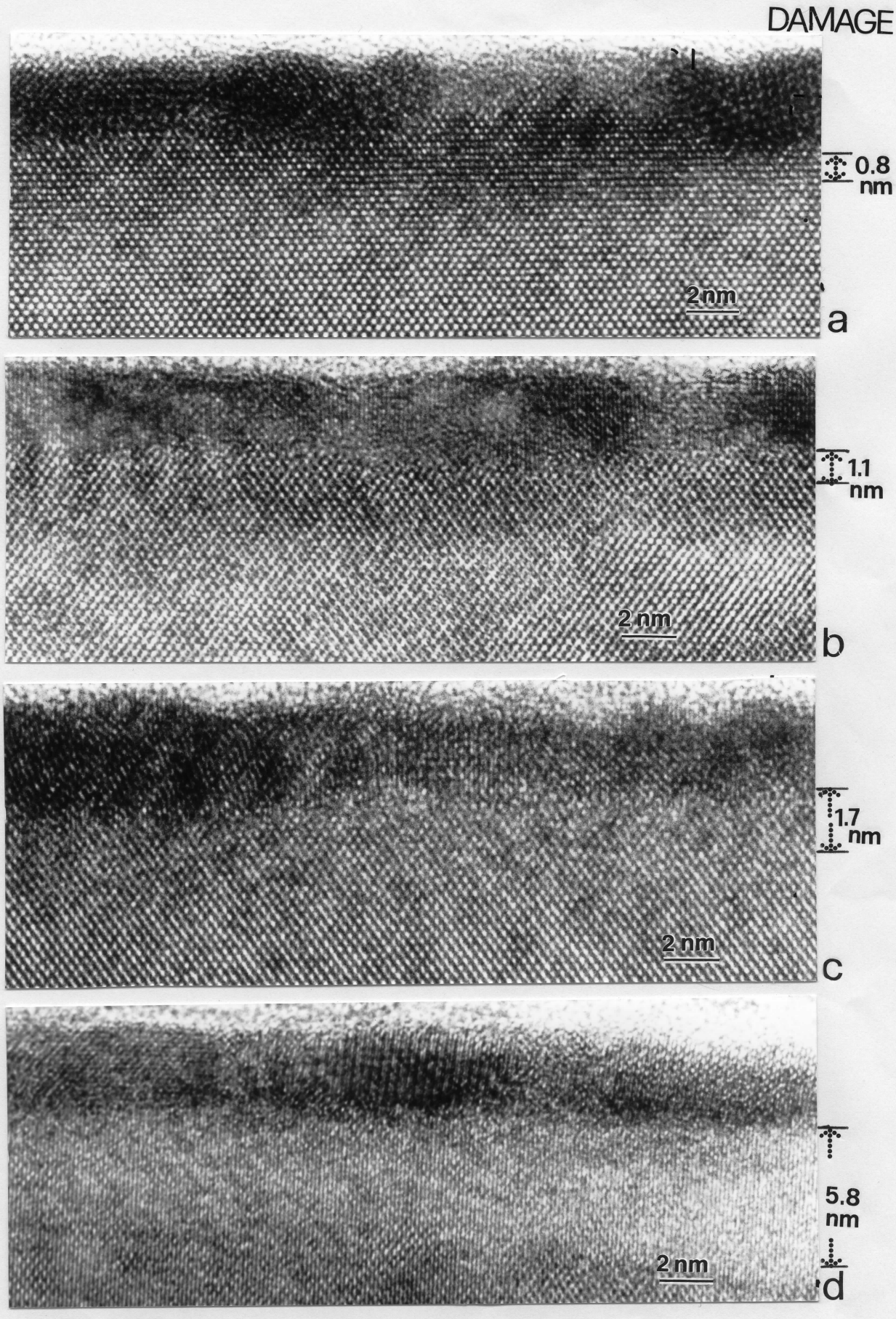


Fig. V.15i: HRTEM cross-sectional images of 550°C-annealed samples: a) N; b) O; c) P; d) Q.

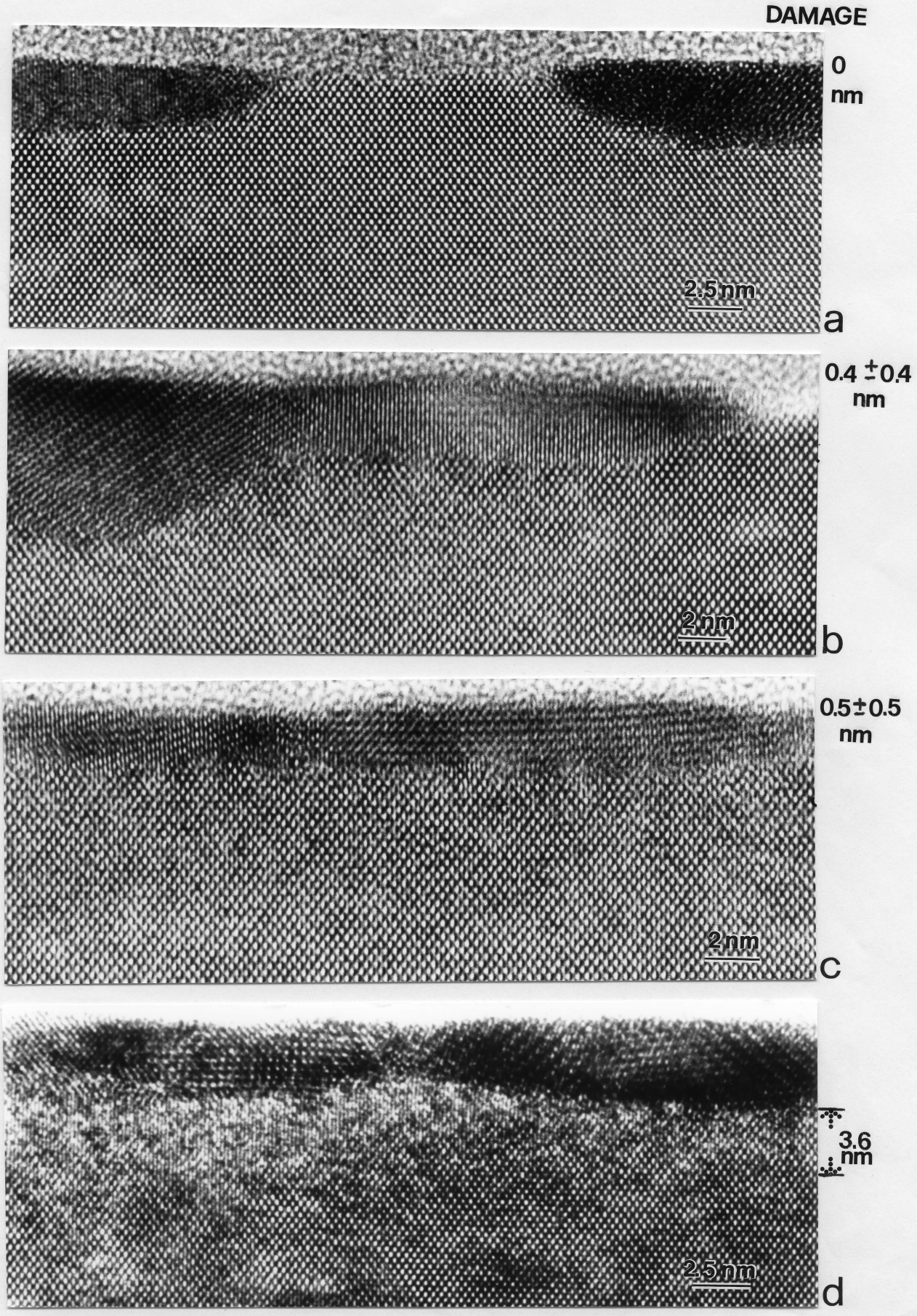


Fig. V.15ii: HRTEM cross-sectional images of 600°C-annealed samples: a) N; b) O; c) P; d) Q.

paragraph we investigate the causes which determine the evolution of the silicide film morphology between 550 and 600 °C.

In the previous section we correlated plasma etching damage depth and the temperature in which film discontinuity is observed. We examine below another aspect of the plasma etching damage: the Si lattice recrystallization and its influence on the silicide film epitaxy.

Figure V.15i and V.15ii show cross-sectional images at 550 and 600 °C annealing temperature of the same samples analyzed by planar-view and ED in Fig. V.14. Samples annealed at 550 °C, in Fig. V.15i, show continuous silicide films formed by epitaxial grains connected by polycrystalline grains. Some amorphous Pt + Si can also be seen between two epitaxial or between randomly-oriented/epitaxial grains. The plasma etching damage on the Si substrate surface has partially annealed in all samples. This means that Si lattice has re-grown from the bottom of the damaged region. Because of this, the damaged region seems less deep in a 550 °C-annealed sample than in the same as-deposited samples . In particular, we can observe some regions, as in sample N (Fig. V.15ia) where the annealing of the Si substrate lattice progressed into the region previously occupied by platinum silicide atomic planes at the substrate surface.

From Fig. V.15i and V.15ii we obtain the 'residual' damage depth at 550 and 600 °C that are shown below:

Sample	Damage depth in as-deposited samples (nm)	Residual damage depth in 550 °C-annealed samples (nm)	Residual damage depth in 600 °C-annealed samples (nm)
M	0.7 ± 0.2	0	0
N	1.5 ± 0.5	0.8 ± 0.3	0
O	1.9 ± 1.0	1.1 ± 0.6	0.4 ± 0.4
P	3.1 ± 1.4	1.7 ± 1.1	0.5 ± 0.5
Q	7.5 ± 1.6	5.8 ± 1.2	3.6 ± 0.7

Table V.2: Plasma etching damage depth at 165, 550 and 660 °C-annealing temperatures.

Micrographs in Fig. V.15ii explain the film discontinuity in planar-view images: the recrystallized silicon lattice reaches the substrate surface between epitaxial grains. In sample N and O (Fig. V.15iia and 15iib), grains are completely isolated or grouped by two or of most three. Comparing with Fig. V.14, we verify that these groups of grains represent the micelle-type film configuration in cross-sectional view. The epitaxy explains the directionality of these grains on the substrate: only precise positions with respect to the substrate surface are allowed to them. Randomly-oriented grains have already been incorporated in to the large grains. Grains that show an epitaxial relationship with the substrate, as in micelles, are more stable and their atoms require more energy to diffuse to the large grains. Films that form micelles before reaching the discontinuity show a slow rate for resistivity increase, that starts at 500 - 550 °C annealing temperature. The 'micelle' structure, reached after annealing at 600 °C, corresponds to a resistivity value of ~ 1mΩcm. On the

other hand, as we will see in the next paragraph, films that mantain the continuity up to higher temperatures and become discontinuous suddenly do not form micelles.

In sample P (Fig. V.15iic), we find a mix of two situations: some regions where we see recrystallized silicon and discontinuity and other regions with residual plasma damage where the film remains continuous. This is the reason why micelles are less separated in sample P than in sample N (as we saw in Fig. V.14c). The two different regions are present simultaneously due, probably, to inhomogeneities in the initial plasma etching damage depth.

On the other hand, film continuity is observed in sample Q micrograph (Fig. V.15iid) above the residual plasma damage on the silicon surface. The 600 °C-annealed sample Q is quite similar to the same sample annealed at 550 °C, showing epitaxial grains connected by polycrystalline grains or even by residual amorphous Pt + Si. This as-deposited sample show the deepest substrate damage depth and it still shows a residual plasma etching damage (3 ± 1 nm) at 600 °C. The stability of this structure is related to the residual damage, still present at 600 °C. It is the sample that shows the lowest resistivity and the only still useful for electrical conduction after annealing at 600 °C.

The silicide film that shows the lowest resistivity at 600 °C *keeps its polycrystalline and epitaxial grains structure up to this temperature.*

Csepregi et al. ([Csepregi 1975]; [Csepregi 1976]) reported that the Si recrystallization starts of 525 °C. They found a linear Si[100] regrowth in time at 550 °C, reaching 9 nm/min. We also observe Si recrystallization at 550 °C but at a lower rate than Csepregi, as we will see in the next paragraph. Only one of our samples, which has the shallowest damage in as-deposited conditions, shows

complete recrystallization at this temperature. The silicide films become, simultaneous, epitaxial and discontinuous. The same phenomena occur in samples with deeper substrate damage, but at a temperature 50 °C higher. Si anneals with the increase of temperature and, if the damage is shallow, the substrate lattice recrystallization is complete below 600 °C. Figure V.16 shows a plot of the damage annealing (or the reduction of damage depth, in Å) against 1/T for samples O, P and Q. We can observe that the recrystallization rate and the energy activation for the process (obtained by an Arrhenius plot) is different for depths larger than 30 Å (E_{act} = 0.6 eV) or smaller than 10 Å (E_{act} = 1.3 eV). Si needs more energy to recrystallize the 10 Å in the vicinity of the platinum silicide film due probably to the stress caused by the film.

Si recrystallization induces PtSi grain recrystallization establishing an epitaxial relationship.

In the presence of lattice damage in the substrate, grains do not have a preferential orientation and the film remains polycrystalline and continuous. As soon as lattice damage in the substrate has been annealed, the silicide grains re-order to reach epitaxy and the film tends to electrical and morphological discontinuity.

We observe that the silicide films with good transport properties at 600 °C are those which maintain an certain amount of plasma etching damage at the substrate surface.

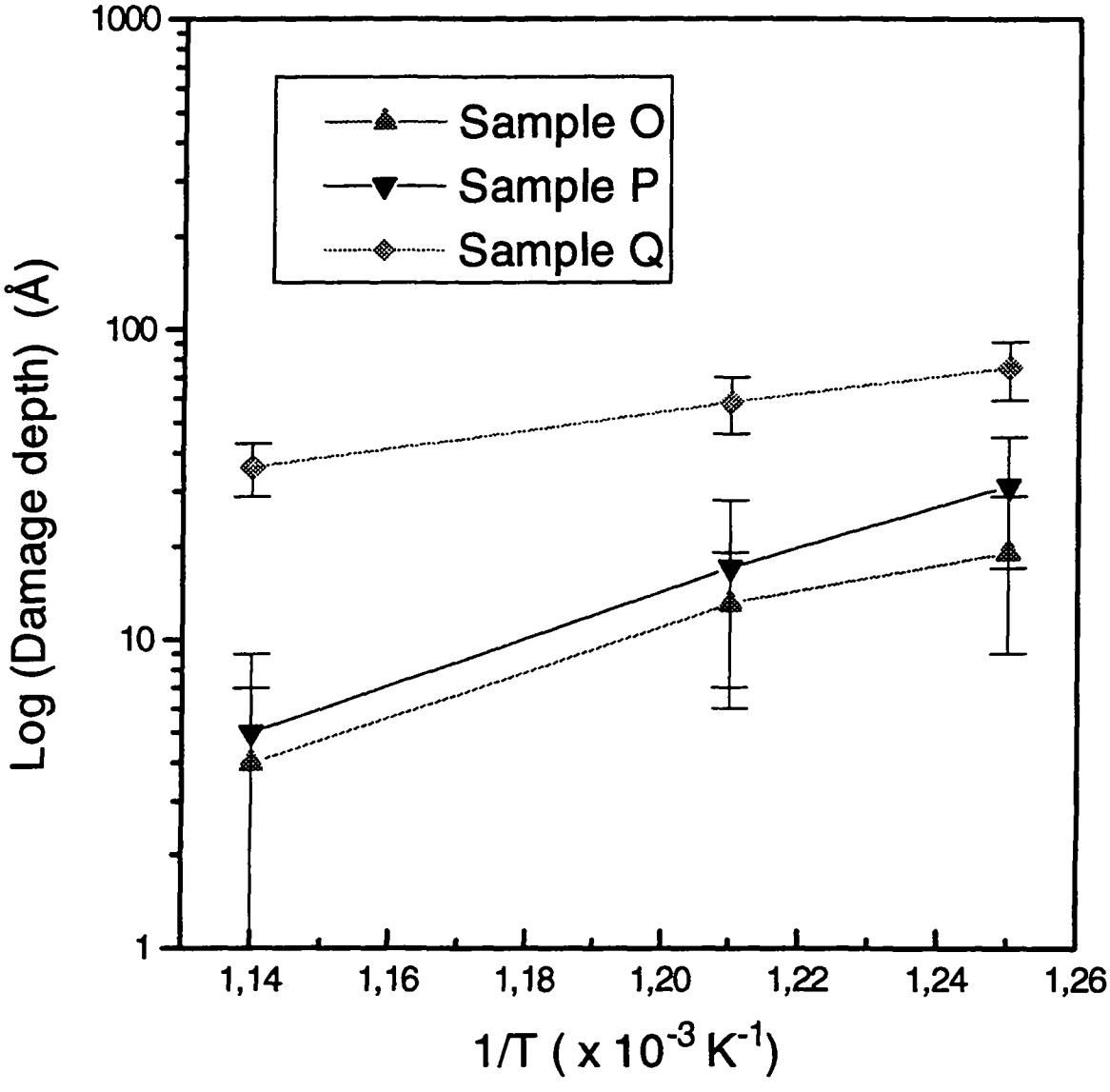


Fig. V.16 - Reduction of the damage depth as a function of the annealing temperature for samples O, P and Q.

Therefore, we can present the following correlation:

Si recrystallization	→	epitaxial PtSi film	→	discontinuous PtSi film
		(increasing PtSi resistivity)		(substrate resistivity)

These results are also valid for 4 - 5 nm PtSi films. In this case, the discontinuity occurs at higher temperature (some tens of degrees). Somewhat paradoxically, an intentional, amount of substrate damage leads to a continuous PtSi/Si interface up to 600 °C. On the contrary, an excessively perfect substrate helps the silicide grains reach their equilibrium shape (isolated grains) even at moderate annealing temperatures and leads to discontinuous, technologically useless, films.

Another interesting feature of our samples is a crystalline/amorphous interface, often observed in films thicker than 4.0 nm. These films can be crystalline at the bottom, at the vicinity of the substrate surface, and amorphous at the top. Thicknesses larger than 4.0 nm allow the progressive silicide film crystallization. Thinner films (thickness < 3.5 nm) do not show this interface: films are amorphous at low temperatures or formed by single-domain grains at medium/high temperatures. We can suppose that the six or seven silicide atomic layers which form these films do not represent a sufficient thickness to support an interface and also that the crystallization progresses quickly through the six or seven layers.

In Fig. V.17 we show an example of each situation: sample B (2.5 nm-deep plasma etching damage), annealed at 250 °C, shows polycrystalline and epitaxial PtSi regions (grains are not well-defined), but only near the silicide/Si interface. The upper part of the same layer is amorphous. Sample N (plasma etching damage depth of 1.5 nm) annealed at the same temperature, shows only amorphous silicide. In Fig. V.18 we can observe the same sample annealed at 550 °C. This film is fully

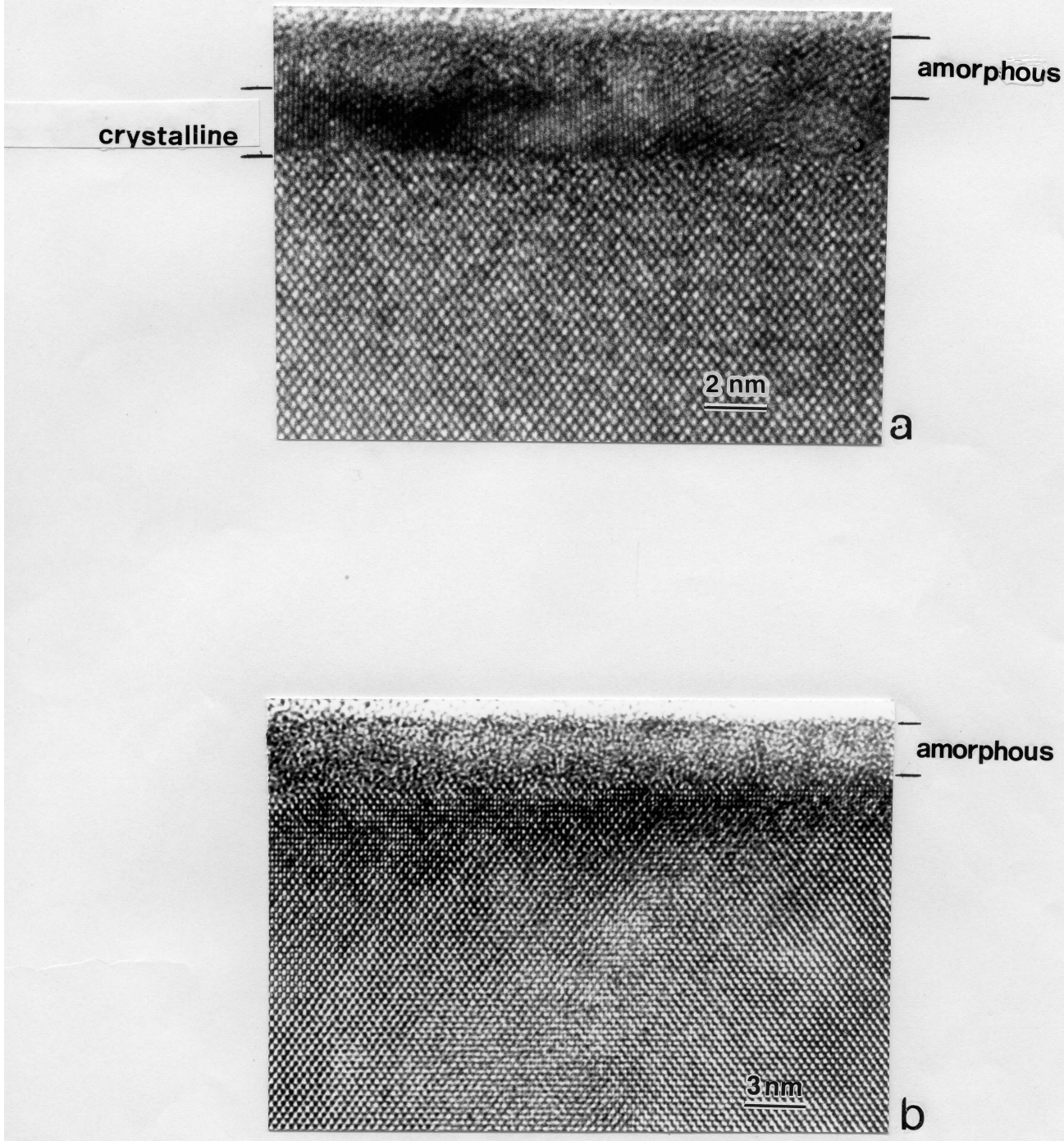


Fig. V.17: HRTEM cross-sectional images of 250°C-annealed samples: a) B; c) N.

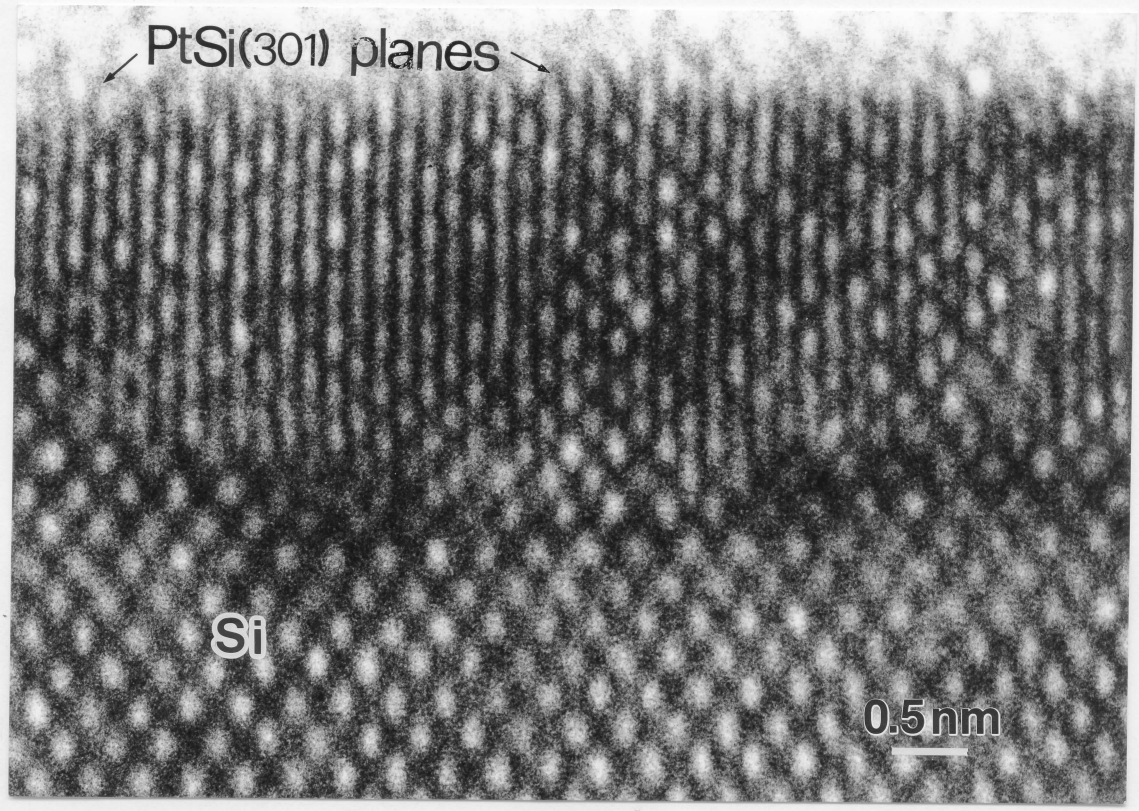


Fig. V.18: HRTEM cross-sectional image of sample O annealed at 600°C, showing PtSi(301) planes parallel to Si(220) planes.

crystallized and we can see a grain formed by atomic PtSi planes in [301] direction, which have $d \sim 0.17$ nm and are parallel to Si(220) planes.

V.4 Conclusions

- 20 nm-thick silicide films on Si(100) with or without an interfacial silicon oxide layer (1.3 - 2.2 nm-thick) are equivalent, for practical applications, in the 250 - 550 °C annealing temperature range. The maximum annealing temperature to obtain a resistivity of $\rho \sim 3 \times 10^{-5}$ Ωcm ($R_s \sim 15$ Ω/□) is 550 °C for samples with interfacial oxide and 600 °C for samples without interfacial oxide layer. If resistivities of (8-10) x 10^{-5} Ωcm ($R_s \sim 40$ - 50 Ω/□) are accepted, the maximum safe annealing temperature can be as high as 650 °C.

- Among silicide films of equal thickness, samples without plasma etching substrate damage show a resistivity increase starting at lower temperatures than those with some amount of plasma damage on the substrate. This resistivity increases corresponds to the outset of the silicide segregation of into isolated islands.

- (4 - 5) nm-thick silicide films show a resistivity increase starting from higher temperatures (600 °C) with respect to the thinner (2.9 - 3.5 nm) ones (550 °C).

- For (4 - 5) nm-thick samples we found the following compromise between resistivity and maximum temperature annealing:

- if resistivities as low as $\rho \leq 8 \times 10^{-5}$ Ωcm ($R_s \leq 160$ Ω/□) are needed, the best procedure is not to use plasma etching bombardment. The maximum annealing temperature can not exceed 500 °C;

- if resistivities between $1.8 \leq \rho \leq 2.5 \times 10^{-4}$ Ωcm ($350 \leq R_s \leq 500$ Ω/□) are acceptable, the plasma etching before metallic film deposition is recommended, and the maximum safety annealing temperature is 600 °C. The safety conditions for plasma etching bombardment is 100 W during 2 minutes, in order to obtain a few nanometers as plasma etching damage depth in the substrate surface. The Si lattice damage depth should not extend beyond a few nanometers below the interface if the properties of the junction have to be preserved.

- For (2.9 - 3.5) nm-thick samples, we can obtain the smallest resistivity ($\rho = 1.5 \times 10^{-4}$ Ωcm or $R_s \sim 400$ Ω/□ at 550 °C) and the maximum safety annealing temperature (600 °C) using 100 W during 2 minutes as plasma etching bombardment. As in the 4.0 nm-thick films case, the aim is to obtain a few nanometers as damage depth.

- Films that show a good and stable transport properties are constituted by randomly oriented and/or epitaxial grains.

- The resistivity increase, as a function of the annealing temperature, can be slow or fast depending on the plasma etching damage depth. In the slow increasing process, the film can reach a micelle-type morphology, that shows resistivity of ~ 1 mΩcm.

REFERENCES

[Abelson 1988] R. Abelson, K.B. Kim, D.E. Mercer, R. Helms, R. Sinclair and T.W. Sigmon, J. Appl. Phys. **63**(3), 689 (1988).

[Csepregi 1975] L. Csepregi, J.M. Mayer, and T.W. Sigmon, Phys. Lett. **54A**(2), 157, (1975);

[Csepregi 1976] L. Csepregi, E.F. Kennedy, S.S. Lau, J.M. Mayer and T.W. Sigmon, Appl. Phys. Lett. **29**(10), 646, (1976).

[Koenecke 1981] C.J. Koenecke, S.M. Sze, R.M. Levin, and E. Kinsborn, paper 15.6, IEEE Electron Device Meeting, Washington, D.C., Dec. 1981.

[Murarka 1983] S.P.Murarka, "Silicides for VLSI Applications", Academic Press, 1983.

[Sinha 1972] A.K. Sinha, R.B. Marcus, T.T. Sheng and S.E. Haszko, J. Appl. Phys. **43**(9), 3637 (1972).

[Sze 1981] S.M. Sze, "Physics of Semiconductor Devices", 2nd edition, Wiley Interscience (1981).

[Sze 1985] S. Sze, "VLSI Technology", McGraw-Hill Book Co., 3rd ed., (1985).

CHAPTER VI

CONCLUSIONS

Silicide films with interfacial oxide layer up to 2.2 nm-thick, annealed at an appropriate temperature, are equivalent to oxide-free samples for application in device metallization. This conclusion is based on resistivity measurements that show the same minimum value, 30 μΩcm, for samples with and without interfacial oxide in the 350 - 550 °C annealing temperature range.

The role played by the interfacial native oxide layer is observed during the early stages of Pt - Si formation. In the absence of the interface oxide, Pt reacts easily with Si and some platinum silicide forms at low temperatures (< 200 °C). If an interfacial oxide is present, the reactant interdiffusion proceeds through the oxide pinholes; the Pt-Si reaction speed and the sequence of phase formation mostly depend on the pinhole density and diameter. For a 1.3 nm-thick oxide, the silicide formation process is quite similar to that of ans oxide-free sample. A 2.2 nm-thick oxide (with low pinhole density) is enough to slow down the Pt supply and change the silicide formation process. The resistivity, on the other hand, is moderately sensitive to these differences in the silicidation process; we observe small differences in the resistivity evolution of the silicide films with or without oxide with temperature increasing up to 250 °C. Resistivity values remain of the same order of magnitude.

By increasing the annealing temperature to the 350 - 550 °C range, silicide films with or without interfacial oxide layer reach a stable, homogeneous and quite similar structure, formed by epitaxial and polycrystalline PtSi grains and a very flat silicide/Si interface. Silicide films with interfacial oxide layer keep a continuous Pt_2Si

sub-layer up to higher temperatures, which does not influence their resistivity with respect to oxide-free samples, where the Pt_2Si layer does not exist. *Annealing in the 350 - 550 °C temperature range gives crystallographic and morphollogic conditions in which silicide films with or without interfacial oxide layer show the best transport properties.*

The Pt_2Si sub-layer plays an important role, however, during the transformation that leads to an island-type film, after annealing at 550 - 600 °C. The existence of this sub-layer can guarantee film continuity up to higher temperatures (700 °C), even if PtSi grains are already epitaxial and isolated from each other. Its presence is beneficial and even desirable for good electrical properties.

The transport properties of ultrathin platinum silicide films (thickness < 5 nm) are very sensitive to morphological and crystallographic characteristics of the silicide film. An important role on these characteristics is played by the plasma etching damage on the substrate surface, which varies slightly depending on the thickness range (thicker than 4 nm or thinner than 3.5 nm) of the silicide film. The deeper the damage depth, the higher the temperature at which the Si lattice recrystallization is complete. To preserve junction properties, the damage depth cannot exceed a few nanometers. However, this damage depth is enough to prevent the Si lattice from recrystallizing completely temperatures lower than 600 °C. This allows the silicide film to preserve the film continuity. Thus, it contributes to slowing down the beginning of the island formation in the silicide film. For ~ 5 nm-thick films, a few nanometers of plasma etching damage depth increase slightly the film resistivity with respect to a film without plasma bombardment, but it guarantees film continuity up to 600 °C. Without plasma etching, the maximum temperature at which the film can be annealed without loss of continuity is 500 °C.

Thinner silicide films (2.9 - 3.5 nm-thick) can benefit considerably from a few nanometers of plasma etching damage, with which the smallest resistivity ($(1.5 \pm 0.1) \times 10^{-4}$ Ωcm) and the maximum safe annealing temperature (600 °C) are obtained. With a plasma etching damage shallower than 1 nm, the minimum resistivity value is

three times larger than mentioned above and the maximum safe annealing temperature is 500 °C.

APPENDIX 1

In the first part of this section we present an indexation of ED patterns shown in Chapter IV for the three different kind of samples: sample X, without interfacial oxide layer; sample Y and Z, with 13 Å- and 22 Å-thick interfacial oxide layers. These ED patterns are constituted by rings (indicating polycrystallinity) and spots (indicating epitaxy) originated from silicide phases and unreacted Pt, superposed to spots from Si substrate in [100] zone axis. These rings and spots were identified by numbered arrows in the figures of Chapter IV; numbers corresponding to arrows are placed at left (in italic) in the list below, followed by the corresponding phase and crystallographic direction. This list is organized as tables following the figure numbers of Chapter IV. Not all but the main (or the most intense) rings and spots of each phase identified in each ED pattern are described.

In the second part of this section, we describe the evolution from a randomly oriented structure towards the epitaxy by the appearance of new spots (or re-ordering of rings into spots) as a function of the annealing temperature. Only the re-ordering of the PtSi phase is considered. The PtSi orientation to which the appearing spots belong is also mentioned. All the diffraction patterns were obtained from planar-view samples, i.e., in the direction parallel to Si[100] zone axis.

I) Indexation of ED patterns (Chapter IV):

1) Sample X as-deposited (Figure IV.1c):

Phase	Unreacted Pt	$Pt_{12}Si_5$	Pt_2Si
Arrows and crystallographic indexation	*6* - Pt(111) *8* - Pt(200) *9* - Pt(220)	*1* - $Pt_{12}Si_5$(301) *3* - $Pt_{12}Si_5$(420) *5* - $Pt_{12}Si_5$(440)	*2* - Pt_2Si(101) *4* - Pt_2Si(110) 7 - Pt_2Si(112)

2) Sample Y as-deposited (Figure IV.2c):

Phase	Unreacted Pt	Pt_2Si
Arrows and crystallographic indexation	*3* - Pt(111) *5* - Pt(200) *7* - Pt(220)	*1* - Pt_2Si(101) *2* - Pt_2Si(110) *4* - Pt_2Si(112) *6* - Pt_2Si(202)

3) Sample Z as-deposited (Figure IV.3c):

1 - Pt(111); ring

2 - Pt(200); ring

3 - Pt(220); ring

4) Sample X annealed at 250 °C (Figure IV.4c):

Phase	Pt_2Si	PtSi
Arrows and crystallographic indexation	*2* - Pt_2Si(101) *4* - Pt_2Si(110) *9* - Pt_2Si(112) *12* - Pt_2Si(202)	*1* - PtSi(110) *3* - PtSi(101) *5* - PtSi(111) *6* - PtSi(201) *7* - PtSi(211) *8* - PtSi(121) *10* - PtSi(002) *11* - PtSi(301)

5) Sample Y annealed at 250 °C (Figure IV.5c):

Phase	Unreacted Pt	Pt_2Si
Arrows and crystallographic indexation	*4* - Pt(111) *5* - Pt(200)	*1*- Pt_2Si(101) *2* - Pt_2Si(002) *3* - Pt_2Si(110) *6* - Pt_2Si(202)

6) Sample Z annealed at 250 °C (Figure IV. 6e):

Phase	Unreacted Pt	$Pt_{12}Si_5$	Pt_2Si	PtSi
Arrows and crystallographic identification	*6* - Pt(111) *13* - Pt(220) *14* - Pt(311)	*5* - $Pt_{12}Si_5$(440) *10* - $Pt_{12}Si_5$(501)	*2*- Pt_2Si(101) *15* - Pt_2Si(110)	*1* - PtSi(110) *3* -PtSi(111) *4* - PtSi(210) *7* - PtSi(121) *8* - PtSi(200) *9* - PtSi(310) *11* - PtSi(002) *12* - PtSi(301)

7) Sample X annealed at 550 °C (Figure IV.8e):

1 - PtSi(110)	*4* - PtSi(111)	*7* - PtSi(121)	*10* - PtSi(002)
2 - PtSi(200)	*5* - PtSi(021)	*8* - PtSi(220)	*11* - PtSi(301)
3 - PtSi(020)	*6* - PtSi(211)	*9* - PtSi(310)	

8) Sample Y annealed at 550 °C (Figure IV.9c):

Phase	Unreacted Pt	Pt_2Si	PtSi
Arrows and crystallographic identification	*6* - Pt(111)	*2* - Pt_2Si(002) *3* - Pt_2Si(110)	*1* - PtSi(110) *4* - PtSi(111) *5* - PtSi(210) *7* - PtSi(211) *8* - PtSi(121) *9* - PtSi(220) *10* - PtSi(310) *11* - PtSi(002) *12* - PtSi(301)

9) Sample Z annealed at 550 °C (Figure IV.10c):

Phase	Unreacted Pt	Pt_2Si	PtSi
Arrows and crystallographic indexation	*13* - Pt(220)	*2* - Pt_2Si(101) *3* - Pt_2Si(002)	*1* - PtSi(101) *4* - PtSi(111) *5* - PtSi(210) *6* - PtSi(211) *7* - PtSi(121) *8, 9* - PtSi(220) *10* - PtSi(310) *11* - PtSi(002) *12* - PtSi(301)

10) Sample X annealed at 700 °C (Figure IV.11d):

1 - PtSi(110)	*4* - PtSi(210)	*7* - PtSi(002)
2 - PtSi(101)	*5* - PtSi(121)	*8* - PtSi(301)
3 - PtSi(111)	*6* - PtSi(310)	

11) Sample Y annealed at 700 °C (Figure IV.13d):

Phase	Pt_2Si	PtSi
Arrows and crystallographic indexation	*3* - Pt_2Si(002) *4* - Pt_2Si(110)	*1* - PtSi(110) *2* - PtSi(101) *5* - PtSi(111) *6* - PtSi(210) *7* - PtSi(201) *8* - PtSi(021) *9* - PtSi(211) *10* - PtSi(121) *11* - PtSi(220) *12* - PtSi(310) *13* - PtSi(002) *14* - PtSi(301)

12) Sample Z annealed at 700 °C (Figure IV.14c):

Phase	Pt_2Si	PtSi
Arrows and crystallographic indexation	*13* - Pt_2Si(002) *3* - Pt_2Si (110)	*1* - PtSi(110) *2* - PtSi(101) *4* - PtSi(111) 5 - PtSi(210) *6* - PtSi(201) *7* - PtSi(211) *8* - PtSi(121) *9* - PtSi(220) *10* - PtSi(310) *11* - PtSi(002) *12* - PtSi(301)

13) Sample Z annealed at 800 °C (Figure IV.16b):

Large agglomerates: PtSi[201] orientation

Small agglomerates: PtSi[1,-1,-2] orientation

II) Crystallographic re-ordering as a function of the annealing temperature:

The table below describe the increase of crystallographic order during the evolution from a randomly-ordered structure towards the epitaxy. Only the new spots observed at each temperature are indicated but the spots already observed at lower

annealing temperatures are also present, named as 'previous spots'. All ED patterns were obtained from planar-view preparations, observed in the direction parallel to the [100] orientation of the substrate. The new spots observed in the ED pattern, for each annealing temperature indicate the re-ordering of silicide grains towars the epitaxy. This transformation is not the same for different interfacial oxide thicknesses, but depends on the thickness of the oxide layer.

1) Sample X (oxide-free substrate):

Temperature (°C)	PtSi phase
As-deposited	–
250	Only rings
350	Only rings
450	Only rings
550	spots: (121)*; (220)*; (002)*; (301)*
600	previous spots and: (310)
700	previous spots and: (101); (111)*; (210)*
800	previous spots

* spots also seen by Ghozlene et al. [Ghozlene 1978]

Table 1: Crystallographic evolution of the silicide film with the increase of temperature for sample X.

2) Sample Y (13 Å-thick interfacial oxide layer):

Temperature (°C)	PtSi phase
As-deposited	–
250	–
350	Only rings
450	spots: (111)*; (210)*; (120)**; (121)*; (002)*; (130)**
550	previous spots and: (001)*
600	previous spots
700	previous spots and: (110)*; (101); (201)**; (211)**; (310)**; (301)*
800	previous spots and : (200)**; (021)**; (112)**; (022)**; (231)**; (330)**; (411)**; (141)**

* spots also seen by Ghozlene et al. [Ghozlene 1978]

** spots distributed over a circle (pattern type 2, in Chapter III), indicating texture

Table 2: Crystallographic evolution of the silicide film with the increase of temperature for sample Y.

At 450 °C we observed the first spots, indicating epitaxy, that belong to two PtSi orientations: [1,-2,1] and [1, -1,0] [Ghozlene 1978]. There is a slight predominance of [1,-2,1] structure (PtSi(111), (210), and (121)); one spot (PtSi(002)) belongs to [1,-1,0] orientation. In reality, PtSi(111) belongs to both, [1,-2,1] and [1,-1,0] PtSi orientations. At 550 °C, the new spot observed (PtSi(001)) belongs to [1,-1,0] orientation and at 700 °C, both structures are well developed, with the addition of two new spots (PtSi(110), belonging to the [1,-1,0] orientation and PtSi(301), belonging to [1,-2,1] orientation). At this temperature the epitaxy is already reached and there is not a clear predominance of one structure respect to the other.

3) Sample Z (22 Å-thick interfacial oxide layer):

Temperature (°C)	PtSi phase
As-deposited	-
250	spots: (110)*; (111)*; (210)*; (220)*; (002)* ; (301)*
350	previous spots and: (001)*; (101); (201)**; (211)**; (310)**
450	previous spots
550	previous spots and: (211)**; (121)*; (021)**
600	previous spots
700	previous spots
800	large agglomerates: [201] oriented small agglomerates:[1,-1,-2] oriented

* spots also seen by Ghozlene et al. [Ghozlene 1978]

** spots distributed over a circle (pattern type 2, in Chapter III), indicating texture

Table 3: *Crystallographic evolution of the silicide film with the increase of temperature for sample Z.*

REFERENCES

[Ghozlene, 1978] H.B. Ghozlene, P. Beaufrère, and A. Authier, J. Appl. Phys. **49**(7), 3998 (1978).

APPENDIX 2

In this section we describe in detail the ED patterns shown in Chapter V. They were taken from planar-view preparation and observed in the direction parallel to the Si[100] zone axis. The crystallographic evolution shown by samples annealed at 550 °C and 600 °C (Fig. V.14) is analyzed below:

1) 550 °C-annealed samples:

Some similarities found in the ED patterns for these four samples at 550 °C, indicating a common crystallographic configuration, have been pointed out. Typical epitaxial and polycrystalline directions were observed. In particular, some epitaxial directions are found for the four samples. We list them below, with the interplanar distance value (d):

Spots at 550 °C (all samples)	**Rings at 550 °C (all samples)**
PtSi(111)*,** - d = 0.268 nm	PtSi(101) - d = 0.308 nm
PtSi(210)** - d = 0.261 nm	PtSi(121)** - d = 0.2075 nm
PtSi(110)* - d = 0.407 nm	PtSi(002)* - d = 0.1804 nm
	PtSi(220)* - d = 0.1804 nm
	PtSi(301)** - d = 0.1737 nm

* Atomic planes belonging to PtSi[1,-1,0] oriented grains [Ghozlene 1978].

** Atomic planes belonging to PtSi[1,-2,1] oriented grains [Ghozlene 1978].

These spots and rings, common to the four samples, have as a characteristic to belong to two PtSi orientations, [1,-1,0] and [1,-2,1], as for samples in Chapter IV. Both orientations show a close resemblance with a hexagonal pseudo-symmetry [Ghozlene 1978] and are parallel to Si[100] orientation. In particular, PtSi(111) planes belong to both orientations, in which they occupy the same position with respect to the Si(001). In fig. A2.a we can see a projection of PtSi lattice in [1,-2,1] and [1,-1,0] zone axis. A high resolution image simulation of the same PtSi zone axis can be seen in fig. A2.b.

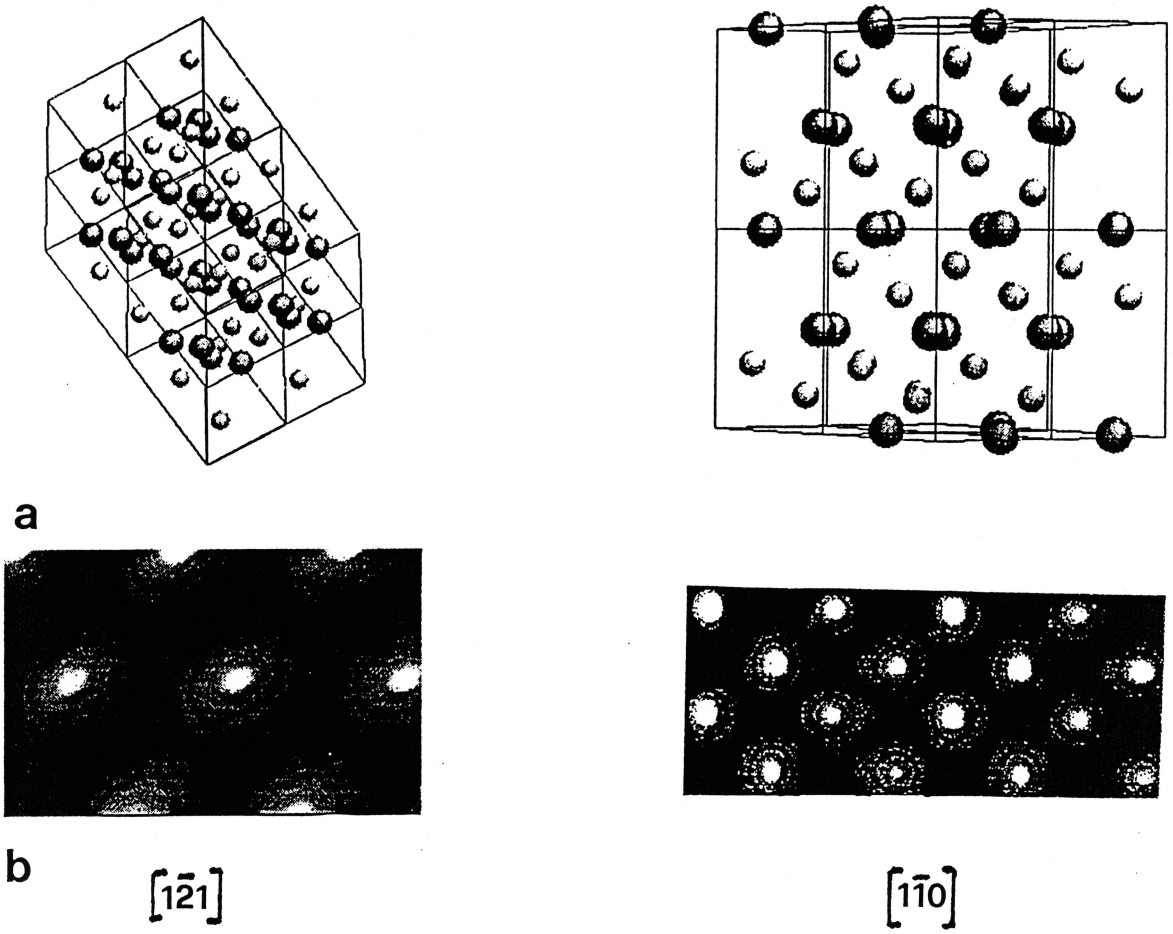


Fig. A2: a) Projection of the PtSi structure in the [1,-2,1] and [1,-1,0] zone axis. b) PtSi simulated image in the same zone axis.

Thus, we found spots, (PtSi(111) and (210)), indicating epitaxy, belonging to two different orientations. On the other hand, in the same ED patterns we find diffuse rings (incoherent reflexion from amorphous silicide) and well-defined rings

(randomly-distributed microcrystals), belonging to the same orientations. In other words, this indicates that the film is mainly polycrystalline, with tendency to order themselves in the orientations mentioned in the above, but not still clearly oriented at this annealing temperature. Thus, neither PtSi[1,-2,1] nor PtSi[1,-1,0] oriented grains are clearly defined and the situation described corresponds to the early stage of the epitaxial growth.

2) 600 °C-annealed samples:

Two different crystallographic configurations are found for 600 °C-annealed samples: micelle-like films and polycrystalline films. Polycrystalline films keep their crystallographic configuration *unchanged between 550 and 600 °C*. Micelle-like films, on the other hand, suffer a crystallographic re-ordering that leads to the epitaxy. Beyond the rings and spots previously mentioned for the 550 °C-annealed samples, we find some additional spots in ED patterns of micelle-like samples annealed at 600 C: PtSi(110), PtSi(121), PtSi(002), PtSi(220) and PtSi(301). All of them were identified as rings (polycrystalline) at 550 °C.

We found well crystallized grains in both orientations, PtSi[1,-2,1] and [1,-1,0] in micelle-like films annealed at 600 °C. We cannot observe a predominance of one orientation with respect to the other. Ghozlene et al found that the predominance of one orientation depends on the thickness of the sample, but they worked with films much more thicker than ours, in the 30 and 70 nm range. For films as thin as ours (3 - 5 nm) the literature does not give any information. Our results show that in these ultra-thin films the two orientations can coexist, without predominance.

REFERENCES

[Ghozlene 1978] H.B. Ghozlene, P. Beaufrère, and A. Authier, J. Appl. Phys. **49**(7), 3998 (1978).

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PUBLICATIONS:

1) E. Conforto, H.R. Rechenberg and M.Jafelicci Jr., "Mössbauer Spectroscopie Study Of The Early Crystallization Stage of IRON(III) Hydroxide Particles", Journal of Physical Chemistry of Solids, **47** (12), 1179-1184 (1986).

2) M. Jafelicci Jr., E. Conforto and F. Galembeck, "Characterization of the Colloidal Products of Pentacarbonyliron Oxidation", Colloids and Surfaces, **23**, 69-81 (1987)

3) E. Nunes Filho, E. Conforto and H. Rechenberg, "Magnetic Ordering Transmission in Amorphous Fe(III) Hydroxide", Journal of Magnetism and Magnetic Materials, **74**, 370-376 (1988)

4) M.T. Furtado, E. Conforto, M.S.S. Loural, A.M. Machado and M.A.Sacilotti, "Characterization of Deep Radiative Levels in GaAlAs Grown by MOVPE", Proceedings of the Third International Brazilian School in Semiconductor Physics (1989).

5) Tiziana dell'Orto, J. Almeida, C. Coluzza, E. Conforto, Gelsomina DeStasio, G. Margaritondo, G. Paic, A. Braem, F. Piuz and B.P. Tonner, 'Laterally Resolved Measurements of Cesium Iodide Quantum Yield', J. Vac. Sci. Tech. **A 13**(6), 2787, (1995).

6) J. Almeida, A. Braem, A. Breskin, A. Buzulutskov, R. Chechik, S. Cohen, C. Coluzza, E. Conforto, G. Margaritondo, E. Nappi, G. Paic, F. Piuz, Tiziana dell'Orto, T. Scognetti, S. Sgobba and B.P. Tonner, 'Microanalysis Surface Studies and Photoemission Properties of CsI Photocathodes', to be published in Nucl. Instr. and Meth. in Phys. Research A (1995).

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CONFERENCES

1) E. Conforto, A. Catana, P.E. Schmid et F. Lévy, 'Microscopie Electronique à Haute Résolution de Films Minces de Siliciure de Platine Recuits à Haute Temperature', Societé Suisse de Physique, Réunion de printemps, Mars 1993, Neuchâtel. **Présentation Orale.**

2) E. Conforto et P.E. Schmid, "Réaction de couches nanométriques de Pt sur Si", Societé Suisse de Physique, Réunion de printemps, Mars 1994, Berne. **Présentation Orale.**

3) E. Conforto and P.E. Schmid, "Reactions of Nanometric Pt Layers on Si by HRTEM", 13th International Congress on Electron Microscopy, Section M2 (Interface Structures), Juillet 1994, Paris, France. **Présentation de Poster.**

4) E. Conforto and P.E. Schmid, "Thin PtSi Films: When Reduced Atomic Mobility Improves Film Quality", Materials Research Society, Fall Meeting, Symposium D (Atomic Level Control of Epitaxial Heterostrucutres), Nov.-Déc. 1994, Boston, Massachusetts, USA. **Présentation de Poster.**